

Modified Absolute Sinusoidal PWM Control of a Self-Balanced 17-Level Switched-Capacitor Inverter with Asymmetric Capacitor Voltages

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Abstract:

A 17-level switched-capacitor inverter is presented in which four capacitors are held at two different voltages, two at the input voltage and two at half of it, so that the smallest voltage step the converter can synthesise is 23.59 V from a 47.175 V source. The structure delivers seventeen levels and a fourfold voltage gain from fourteen switches, four capacitors, two diodes and one DC source, twenty main power components in all, which gives a component-to-level ratio of 1.18 and a cost function of 2.38. Balancing is inherent, so no voltage sensor, no balancing controller and no redundant-state selection are required. The converter is driven by modified absolute sinusoidal PWM, whose eight switching angles are computed before the converter runs, so each device commutates twice per fundamental cycle rather than the 200 times a 10 kHz carrier would demand, and the switching loss is held to 0.07 W of a 1.88 W total. Simulation returns a fundamental of 187.7 V, an output of 132.7 V rms and a voltage distortion of 2.53%. An FPGA-controlled prototype supplying a 180 W single-phase induction motor at a power factor of 0.76 returned 186.7 V, 132.3 V rms, a gain of 3.96 against the ideal 4.00, a measured voltage distortion of 2.9%, a measured current distortion of 2.8% and an efficiency of 94.6%, with capacitor ripples between 2.3% and 4.5% and no device stressed above 143.3 V. The total standing voltage is 1073.6 V, that is 5.69 per unit.

Keywords: MASPWM, switched-capacitor inverter, multilevel inverter, self-balancing, total harmonic distortion.

1 INTRODUCTION

Multilevel inverters have moved from laboratory curiosities to the default choice in photovoltaic plants, motor drives and electric vehicles. The reason is simple enough: a staircase built from many small steps sits closer to a sinusoid than a square wave ever will, so the filter shrinks, the devices see less voltage and the radiated interference drops (Munawar et al., 2024; Vemuganti et al., 2021).

Each classical family pays for its levels in a different currency. Neutral-point clamped converters pay in

clamping diodes and in the circuit that keeps the DC-link split balanced (Taghvaie et al., 2020). Flying-capacitor converters pay in pre-charging hardware and in capacitors whose voltages must be tracked at switching speed (Kampitsis et al., 2022). Cascaded H-bridges avoid both problems and then ask for an isolated source per cell, which no single photovoltaic string can provide (Singh et al., 2024). Hence the long search for structures that yield more levels from fewer parts (Gupta et al., 2016; Vijeh et al., 2019).

Switched-capacitor converters answer part of that. One source charges a set of capacitors, the switching pattern then stacks them in series, and the output rises above the input while the capacitor voltages settle on their own with no sensor in the loop (Barzegarkhoo et

al., 2022; Dhanamjayulu et al., 2021). The bill arrives elsewhere: more switches, uneven blocking voltages, and a start-up current that is limited only by wiring resistance until something is put in its way, usually a resistor, a series inductor or a resonant charging branch (Poulad et al., 2025; Memis and Karakilic, 2025).

The recent 17-level converters show where the field stands, and each shows the same ceiling from a different angle. Sun et al. (2022) draw seventeen levels from sixteen switches, but the gain stops at two. Haghighian et al. (2023) and Mansourizadeh et al. (2025) reach three, again with sixteen switches and extra diodes. Marangalu et al. (2023) trim the count to fourteen switches and still stop at three, now with four diodes. Chandan et al. (2024) push the gain to eight and pay with twenty switches and six capacitors. What ties them together is a habit rather than a device limit: every capacitor is charged to the same voltage, so the smallest step the converter can make equals that voltage, and levels have to be bought one capacitor at a time. Unequal capacitor voltages loosen the constraint, and they have been used at nine levels (Varesi et al., 2022) and in an asymmetric multicell arrangement (Hosseinizadeh et al., 2022), but not yet in a seventeen-level converter with a fourfold gain that still balances itself. That is the opening this work takes.

Modulation is the other half of the problem. A seventeen-level carrier scheme wants sixteen carriers and a comparator bank, and it asks every device to commute a few thousand times a second. The modified absolute sinusoidal PWM technique of Antar (2018), later carried into other control structures (Antar, 2024) and into harmonic mitigation for PV-fed asymmetric inverters (Ali et al., 2023; Ali et al., 2024), goes the other way. The angles come from the absolute value of the reference and are worked out before the converter runs, so each device changes state once per half-cycle and the zero level disappears from the waveform. No carriers, no comparators, no kilohertz gating. For a converter that already carries fourteen switches, that matters.

Two things separate this work from the seventeen-level converters already published. The first is structural. Every switched-capacitor design in that group charges all of its capacitors to the same voltage, which fixes the smallest synthesisable step at that voltage and ties each further level to a further capacitor and switch pair. Holding two capacitors at the input voltage and two at half of it halves the step instead, so four capacitors reach seventeen levels where a symmetric arrangement of the same four would reach nine. The second is the modulation, and

it is the one the title carries. The comparable converters are driven by multicarrier schemes that commute every device a few thousand times a second; here the eight switching angles are computed before the converter runs, each device changes state twice per fundamental cycle, and the measured consequence is a switching loss of 0.07 W in a 1.88 W budget, under 4% of the total. On component count the proposed converter is not the smallest of the group, as Table 10 shows plainly, and no claim is made that it is; what it offers is a fourfold gain and a filterless 2.9% measured distortion obtained at fundamental switching frequency, with inherent balancing and no sensor, verified on a real induction motor rather than on a resistive-inductive load.

This paper puts the two together. Two capacitors are held at the input voltage, two at half of it, and the whole converter runs on MASPWM at 50 Hz. Four things come out of it. The power stage makes seventeen levels and a fourfold gain from fourteen switches, four capacitors and two diodes, and it balances without a single sensor. The gating is done on an FPGA with eight stored angles and a level decoder, which is all the asymmetric structure needs. The balancing is proven analytically, and the capacitors and the soft-charging inductor are sized from the maximum discharge duration rather than by rule of thumb. Finally the design is measured, not only simulated, on a 180 W single-phase induction motor at a lagging power factor, and then set against the reported seventeen-level switched-capacitor converters component by component. Sections 2 and 3 cover the power stage and the modulation, Section 4 the setup, Section 5 the results, Section 6 the conclusions.

2 PROPOSED 17-LEVEL SC-MLI TOPOLOGY

Before the circuit is described it is worth saying why seventeen levels are worth their switch count, since the count is the first thing a reader notices. Three things decide it. The first is distortion: the harmonic content of a staircase falls as the number of levels rises, and seventeen levels bring the output to 2.53% in simulation and 2.9% in measurement with no output filter at all, where a nine-level version of the same structure would roughly double the step and the distortion with it and would need a filter whose inductor and capacitor carry their own loss, volume and cost. The second is that the fourteen switches are not all expensive ones. The blocking voltages are

graded over a four-to-one range, so only four positions need devices rated above 100 V while the other ten take cheaper low-voltage parts with lower on-state resistance, and the measured conduction loss comes to 0.62 W. A converter with fewer but uniformly stressed devices does not automatically cost less. The third is that switching loss does not follow the switch count under the modulation used here. Because the angles are precomputed and every device commutates once per half-cycle, the total switching loss is bounded at 0.07 W in a 1.88 W budget, under 4%, so the extra devices cost conduction loss, quantified in section 5.3, and almost no switching loss. The fourfold gain completes the answer, because it removes the front-end DC-DC stage a lower-gain converter would need, and that stage would bring its own switches, inductor and losses.

2.1 Circuit Structure and Functional Stages

The power stage is built from one DC source, fourteen bidirectional switches made as back-to-back MOSFET pairs and driven by eleven independent gate signals, four capacitors and two diodes, arranged as in Figure 1. C1 and C2 sit at V_{in} , C3 and C4 at half of it, and between them the converter reaches seventeen levels with nothing measuring the capacitor voltages and nothing correcting them.

Three stages do the work. S1 and S2 at the source terminals set the polarity for each half-cycle. The boosting stage, C1 and C2 with S3, S4, S13, S14 and diode D1, parks the two capacitors in parallel across the source while they charge, through S13-D1 in the positive half-cycle and through S14-D2 in the negative one, then stacks them in series with the source while they discharge. The right-hand stage, C3 and C4 with S5 to S12, forms the divider that pins both capacitors at $0.5V_{in}$, routes the result to the load, and picks either the divider midpoint or the whole divider depending on the level being made.

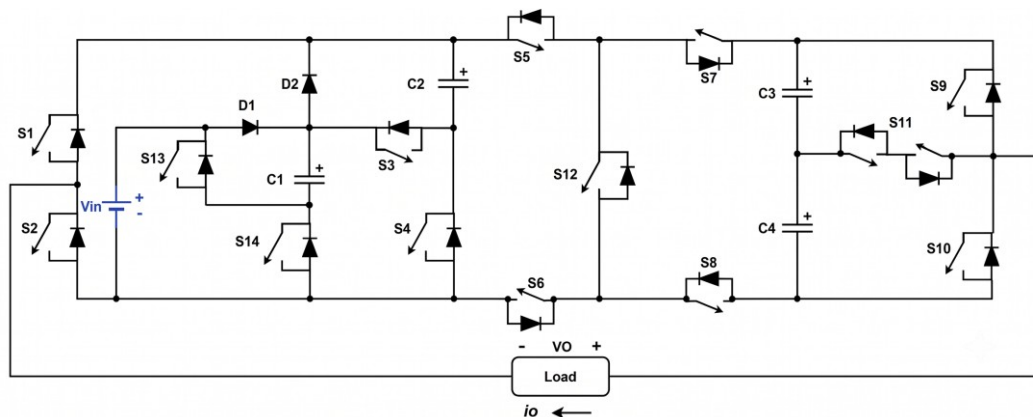


Figure 1: Proposed 17-level SC-MLI topology.

2.2 Asymmetric Capacitor Voltage Distribution

The ratio written as 1:1:0.5:0.5 needs a word of definition, because it is a ratio of steady-state capacitor voltages and not of capacitances. It states that $VC1 : VC2 : VC3 : VC4 = V_{in} : V_{in} : 0.5V_{in} : 0.5V_{in}$, that is 47.175 V, 47.175 V, 23.59 V and 23.59 V for the input used throughout this work. The four capacitances are equal, 10 mF each; what differs is the charging path. C1 and C2 are charged directly across the source and reach the full input voltage, while C3 and C4 are connected in series across the

intermediate bus during their charging states, so each receives half of it. The significance of the halved pair is that the smallest voltage increment the converter can add to or remove from the output becomes $0.5V_{in}$ instead of V_{in} , and that is what allows four capacitors to generate seventeen levels where a symmetric arrangement of the same four would generate nine.

Holding the two pairs apart in this way is a design choice, not a by-product. C1 and C2 do the boosting at full voltage, C3 and C4 work at half and hand the converter its $0.5V_{in}$ step, and that step is the whole point, because the smallest increment a staircase can make decides how many levels four capacitors can produce. Capacitance follows from the charge each

capacitor loses during its maximum discharge duration, worked out in section 2.6; one standard value of 10 mF clears the 10% ripple limit for all four, which keeps the parts list short.

Diodes D1 and D2 stop C1 and C2 from bleeding back through the body diodes of the switches while those switches are off (Hussan et al., 2021). Remove D1 and C1 leaks through the body diode of S3 during the high levels, the series sum stops adding up, and the balancing argument of section 2.5 goes with it.

2.3 Switching States and Modes of Operation

Table 1 holds the complete switching pattern, with 1 and 0 for the switch states and C, D and N for a charging, discharging or idle capacitor. Two features deserve a second look: the seven low-magnitude states where all four capacitors are clamped to their source, and the ten high-magnitude states where they

join the string one after another. Four modes are enough to show how it works.

At +0.5Vin the conducting set is S2, S3, S5, S8, S9, S12 and S13. The source charges C1 and C2 in parallel through S13-D1, C3 and C4 charge in series and drift toward half the input each, and the load hangs on the divider midpoint through S9, so the output is 0.5Vin. Most of the recharging happens here.

At +2Vin the set becomes S2, S3, S5, S8, S11, S12 and S14, C1 joins the source in series and the output is Vin + VC1. At +2.5Vin, with S2, S3, S5, S7, S9 and S14 on, C1 and C3 discharge together for Vin + VC1 + VC3, the step no symmetric arrangement of the same four capacitors can produce. At the top level S2, S4, S5, S6, S7, S8, S11 and S14 put the source and all four capacitors in one string for 4Vin.

The negative half is the mirror image. S1 replaces S2, the polarity across the boosting network reverses, and the S13-D1 and S14-D2 paths trade charging duties; nothing else changes.

Table 1: Switching states of the proposed 17-level SC-MLI.

Level	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	C1	C2	C3	C4
+8	0	1	0	1	1	1	1	1	0	0	1	0	0	1	D	D	D	D
+7	0	1	0	1	1	1	1	1	1	0	0	0	0	1	D	D	D	N
+6	0	1	0	1	1	0	0	1	0	0	1	1	0	1	D	D	D	D
+5	0	1	1	0	1	0	1	0	1	0	0	0	0	1	D	N	D	N
+4	0	1	1	0	1	0	0	1	0	0	1	1	0	1	D	N	N	N
+3	0	1	1	0	1	0	0	1	1	0	0	1	0	1	C	N	D	N
+2	0	1	1	0	1	0	0	1	0	0	1	1	1	0	C	C	C	C
+1	0	1	1	0	1	0	0	1	1	0	0	1	1	0	C	C	C	C
0	0	1	0	1	1	1	1	1	0	1	0	0	0	1	C	C	C	C
-1	1	0	0	1	1	1	1	1	0	0	1	0	0	1	C	C	C	C
-2	1	0	0	1	1	1	1	1	0	1	0	0	0	1	C	C	C	C
-3	1	0	0	1	0	1	1	0	0	0	1	1	0	1	C	D	N	N
-4	1	0	1	0	0	1	0	1	0	1	0	0	0	1	D	N	N	N
-5	1	0	1	0	0	1	1	0	0	0	1	1	0	1	D	D	N	N
-6	1	0	1	0	0	1	1	0	0	1	0	1	0	1	D	D	D	D
-7	1	0	1	0	0	1	1	0	0	0	1	1	1	0	D	D	D	N
-8	1	0	1	0	0	1	1	0	0	1	0	1	1	0	D	D	D	D

C = charging, D = discharging, N = idle capacitor.

2.4 Voltage Gain

The peak arrives when the source and all four capacitors form one series string. Kirchhoff along that path gives (1), and the nominal voltages substituted into it give (2).

$$V_o = V_{in} + V_{C1} + V_{C2} + V_{C3} + V_{C4} \quad (1)$$

$$V_o = V_{in} + V_{in} + V_{in} + \frac{V_{in}}{2} + \frac{V_{in}}{2} = 4V_{in} \quad (2)$$

No symmetry assumption enters anywhere, and the gap between neighbouring levels, 0.5Vin, is exactly

what C3 and C4 hold. Table 2 checks every level against the switching states of Table 1.

Table 2: Verification of the output voltage levels.

Level	Expression	Result
±1	± (C3–C4 midpoint)	±0.5Vin
±2	± Vin	±1.0Vin
±3	± (Vin+VC3)	±1.5Vin
±4	± (Vin+VC1)	±2.0Vin
±5	± (Vin+VC1+VC3)	±2.5Vin
±6	± (VC1+VC2+VC3+VC4)	±3.0Vin
±7	± (Vin+VC1+VC2+VC3)	±3.5Vin
±8	± (Vin+VC1+VC2+VC3+VC4)	±4.0Vin

2.5 Self-Balancing Analysis

Self-balancing means the capacitor voltages find their nominal values without help. The condition is that each capacitor ends a fundamental period with the charge it started with, written in (3), with the resulting ripple in (4).

$$\Delta Q_{Ck} = \int_0^T i_{Ck}(t)dt = 0 \quad \forall k \in \{1,2,3,4\} \quad (3)$$

$$\Delta V_{Ck} = \frac{\Delta Q_{Ck}}{C_k} \quad (4)$$

Reading Table 1, C1 charges in the levels 0, +/-1, +/-2 and +/-3 and discharges in +/-4 to +/-8, seven states against ten. The sinusoidal reference settles that imbalance: the low levels last longer near the zero crossings than the high ones do near the peak, so the seven charging states move more charge than their count suggests. The correction comes from the parallel connection itself. Let VC1 drift above Vin by a small amount and the charging current reverses, pulling it back while the discharge current, fixed by the load, stays where it was; a drift below Vin is corrected the same way in the other direction. The argument transfers to C2 word for word.

C3 and C4 are always charged together and in series across the intermediate bus, which fixes their sum by (5) and makes their charge increments equal by (6). Any difference between them decays instead of growing, and both settle at half the input. Collecting the four deviations into the energy function (7) says the same thing formally: the function is positive definite, its derivative during the charging intervals is not, so the equilibrium holds for any starting condition inside the operating range (Niazi et al., 2023).

$$V_{C3} + V_{C4} = V_{in} \quad (5)$$

$$\Delta Q_{\text{charge}} = \int_{\text{charge}} i_{C3}dt = \int_{\text{charge}} i_{C4}dt \quad (6)$$

$$V_L(\epsilon) = \frac{1}{2}[C_1\epsilon_1^2 + C_2\epsilon_2^2 + C_3\epsilon_3^2 + C_4\epsilon_4^2] > 0 \quad (7)$$

2.6 Capacitor Design and Inrush Current Suppression

Capacitor sizing starts from the maximum discharge duration, the longest stretch a capacitor supplies the load without being topped up (Taissariyeva et al., 2025). The switching instants that bound those stretches come from (8), the charge lost during them from (9) and (10), and the minimum capacitances from (11) and (12).

$$t_x = \frac{\arcsin\left(\frac{2x-1}{N_L-1}\right)}{2\pi f_0}, N_L = 17 \quad (8)$$

$$\Delta Q_{C1} = 2 \int_{t_4}^{T/2-t_4} I_0 \sin(\omega t - \phi) dt \quad (9)$$

$$\Delta Q_{C3} = \Delta Q_{C4} = 2 \int_{t_3}^{T/2-t_3} I_0 \sin(\omega t - \phi) dt \quad (10)$$

$$C_1, C_2 \geq \frac{2I_0(\cos\alpha_1 - \sin\phi)}{2\pi f_0 V_{in} \Delta V_{\text{ripple}}} \quad (11)$$

$$C_3, C_4 \geq \frac{2I_0(\cos\alpha_2 - \sin\phi)}{2\pi f_0 V_{in} \Delta V_{\text{ripple}}} \quad (12)$$

Behind those expressions sit two assumptions: the load current is sinusoidal at 50 Hz with amplitude I0 and power-factor angle phi, about 40 degrees for this motor, and the switching ripple is smoothed by the machine inductance. A number makes the procedure concrete. With I0 = 0.46 A and NL = 17, equation (8) puts t4 at 1.44 ms, so the MDD of C1 runs from 1.44 ms to 8.56 ms. Over that window (9) gives 4.0 mC of charge, and (11) asks for at least 0.85 mF to hold the ripple at 10% of 47.175 V. The 10 mF actually fitted is roughly twelve times that, which is why the measured ripple in section 5.2 comes out at 2.5%. Table 3 collects the sizing.

Table 3: Capacitor sizing based on the maximum discharge duration.

Cap.	Nominal V	Selected C	MDD interval
C1	V _m =47.175 V	10 mF	t ₄ -T/2-t ₄ (±4±8)
C2	V _m =47.175 V	10 mF	t ₄ -T/2-t ₄ (±4±8)
C3	0.5V _m =23.59 V	10 mF	t ₃ -T/2-t ₃ (+3 to +8)
C4	0.5V _m =23.59 V	10 mF	short (±6, ±8)

Start-up is the awkward moment. The capacitors are empty, the source sees only the on-state resistance, and Vin/Ron works out at about 175 A for Ron = 0.27 ohm, which no device in this class survives. One inductor Lr with a reverse-parallel diode Dr, placed in series with the source, sits in the charging path of all four capacitors and holds that current down. The switching frequency has to stay above the resonance of the Lr-C network, which is (13), and the inductor itself follows from (14) and (15).

$$f_{sw} > f_r = \frac{1}{2\pi\sqrt{L_r C}} \quad (13)$$

$$L_r \geq \frac{1}{(2\pi f_{sw})^2 C} \quad (14)$$

$$L_r = \frac{V_{in}}{4f_{sw}\Delta I_L} \quad (15)$$

With Lr = 0.23 mH the simulated peak drops to about 12 A, matching the charging spikes on S14 in Figure 8. One inductor at the input does the job of four in the

branches, which is a component saved and a loop less to lay out (Poulad et al., 2025).

2.6.1 Resonance and losses in the charging branch

Putting an inductor in a switched-capacitor path raises two questions that deserve numbers rather than assurances. The first is resonance. The branch is a series Lr-C loop, so it rings at $f_r = 1/(2\pi\sqrt{L_r C})$, which for 0.23 mH and 10 mF is 105 Hz. Its quality factor, $Q = (1/R_{on})\sqrt{L_r/C}$, comes to 0.56, that is a damping ratio of 0.89, so the loop is close to critically damped and cannot sustain oscillation. What excites it is not the 50 Hz fundamental but the level transitions, sixteen per half-cycle, about 800 Hz. Since the excitation is roughly eight times the resonant frequency, each charging pulse ends long before the loop can complete a half-oscillation, which is precisely the partial-charging regime the inductor is there to create.

The second question is what the branch itself costs. The inductor carries the charging current, 0.93 A rms in simulation, through the winding resistance; for the hand-wound toroid used here, whose DC resistance measures close to 0.1 ohm, that is 0.09 W. Core loss is negligible at this excitation: the flux swing is small, the fundamental component of the current is at 50 Hz and the ripple content sits near 800 Hz, far below the frequency at which a powdered-iron core of this size begins to dissipate appreciably. The freewheeling diode D_r conducts only while the inductor current decays between charging pulses; with a forward drop of about 1.2 V over that interval it adds roughly 0.03 W. Together the soft-charging branch accounts for about 0.12 W, some 6% of the total loss, which is the price paid to keep the start-up current below 12 A instead of the 175 A the bare resistance would allow.

3 MASPWM CONTROL STRATEGY

3.1 Principle and Switching-Angle Computation

MA SPWM was introduced by Antar (2018) for inverters fed from unequal DC voltages and has since been carried into other control structures (Antar, 2024) and into PV-fed asymmetric topologies (Ali et al., 2023). Rather than compare a reference against a bank of carriers, it works on the absolute value of the reference and computes the switching angles before

the converter is switched on, so every device changes state once per half-cycle.

For NL output levels the angles come from (16); with NL = 17 that gives the eight angles of the positive half-cycle, and the negative half is their mirror image.

$$\theta_i = \sin^{-1} \left(\frac{2i-1}{NL} \right), i=1,2, \dots, \frac{NL-1}{2}=8 \quad (16)$$

Two consequences matter here. All fourteen devices commutate at 50 Hz, not at several kilohertz, which is the practical reason for choosing MASPWM over a carrier scheme that would need sixteen carriers and far more switching events. And the zero level drops out of the waveform, which removes the redundant transitions around the zero crossing and shortens the conduction path in the low levels.

The cost is fixed amplitude. Once NL is chosen the angles are fixed, so the output follows the input and the capacitor voltages rather than a control variable. For a regulated DC link that is no loss.

3.2 Gate-Signal Generation and Implementation

The eight angles sit over the seventeen levels together with the MDD intervals of the four capacitors in Figure 2, and Figure 3 shows the controller as built in MATLAB/Simulink and ported to the FPGA. A comparator bank turns the reference into a level index, a decoder maps that index onto the fourteen gate signals through Table 1, and a complementary path derives the S13 and S14 charging pulses. The decoder is combinational and the angles live in a look-up table, so the whole controller occupies very little logic.

The angles sit in flash and a timer compares elapsed time against them within each half-cycle, following Antar (2024) and Ali et al. (2023). Every complementary pair gets 2 microseconds of dead time to keep the string from shooting through.

4 SIMULATION AND EXPERIMENTAL SETUP

4.1 Simulation Model

The converter, its controller and the motor were modelled in MATLAB/Simulink with the parameters of Table 4: 47.175 V in, 50 Hz out, 10 mF per capacitor, 2 microseconds of dead time, and the same induction motor used on the bench so that simulation

and measurement differ only in what the model leaves out. Recorded quantities are the output voltage and current, their spectra, the four capacitor voltages, and the blocking voltage and current of every switch.

Table 4: Simulation parameters.

Parameter	Value	Parameter	Value
Input voltage V_{in}	47.175 V	Fundamental f_0	50 Hz
Capacitors C_1 – C_4	10 mF / 63 V	Load	180 W motor
Dead time t_d	2 μ s	Modulation	MASPWM (50 Hz)
Switches	IRF100B201	Controller	Spartan-3A FPGA
Gate drivers	TLP358H	Soft-charge L_r	0.23 mH

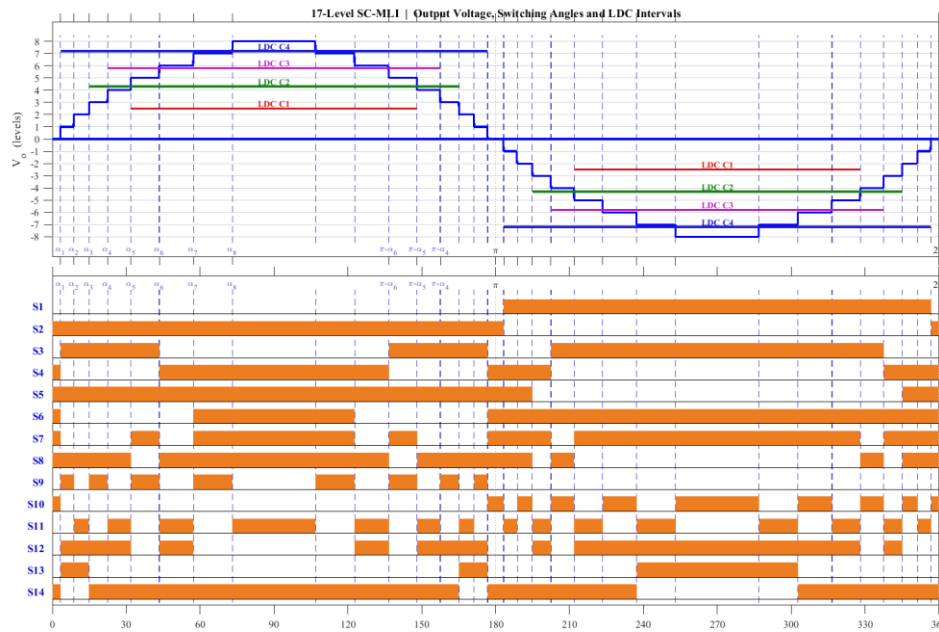


Figure 2: Output voltage levels, MASPWM switching angles and capacitor maximum-discharge-duration intervals.

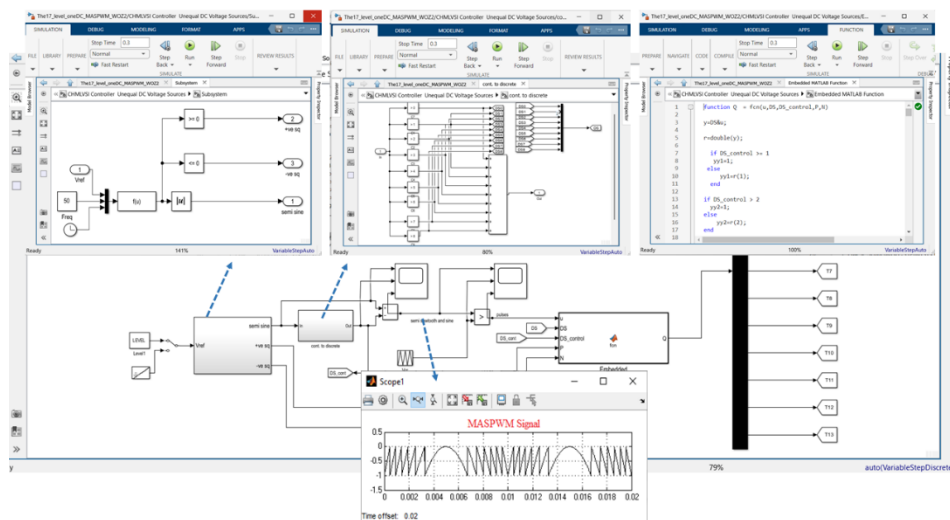


Figure3:MASPWM controller implemented in MATLAB/Simulink: reference generation, level detection, decoder and gate-signal outputs.

4.2 Prototype and Instrumentation

The prototype in Table 5 uses IRFP460 MOSFETs (500 V, 20 A, 0.27 ohm on-state), STTH30L06 blocking diodes (600 V, 30 A), a MUR1560 for the soft-charging branch, a hand-wound 0.23 mH toroid rated at 5 A, and four 10 mF electrolytic capacitors. A Xilinx Spartan-3A DSP FPGA generates the fourteen gate signals and TLP358H optocouplers isolate them.

The load is an off-the-shelf single-phase induction motor: 180 W, 230 V, 1.5 A at full load, 50 Hz, 1400 rpm, with an 8 microfarad run capacitor. A regulated bench source set to 47.175 V feeds the DC side. Waveforms were captured on an FNIRSI DPOS350P digital storage oscilloscope (two channels, 350 MHz bandwidth, 1 GS/s) through compensated 1:10 passive probes. Two channels suffice: the output voltage stays on the first as the trigger reference while the second moves between the load current and one capacitor at a time. Figure 4 shows the bench.

Table 5: Hardware prototype components.

Component	Part / type	Rating	Qty
Power switches S1–S14	IRFP460 MOSFET	500 V / 20 A	14
Blocking diodes D1, D2	STTH30L06	600 V / 30 A	2
Capacitors C1–C4	Electrolytic 105 °C	10 mF / 63 V	4
Soft-charge inductor L_r	Toroid, hand-wound	0.23 mH / 5 A	1
Freewheeling diode D_r	MUR1560	600 V / 15 A	1
Gate drivers	TLP358H optocoupler	2.5 A output	14
Controller	Xilinx Spartan-3A DSP	50 MHz	1

DC supply	Regulated bench supply	0–60 V / 5 A	1
Load	1-ph induction motor	180 W, 230 V, 1400 rpm	1
Oscilloscope	FNIRSI DPOS350P	350 MHz, 1 GS/s, 2 ch	1

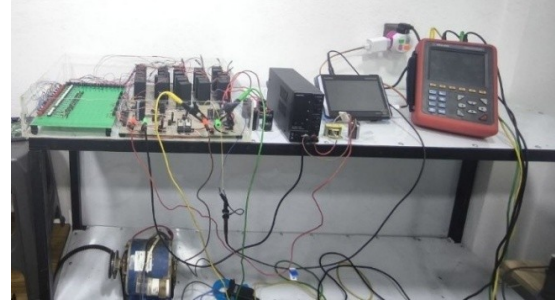


Figure 4: Experimental prototype of the proposed 17-level SC-MLI in the laboratory environment.

5 RESULTS AND DISCUSSION

5.1 Simulation Results

The simulated output is a symmetric staircase of seventeen levels separated by $0.5V_{in} = 23.59$ V, whose peak of 187.7 V is the fourfold boost of the 47.175 V source, while the load current is smoothed by the machine inductance into a near-sinusoid lagging the voltage by the motor power factor. Both are plotted on one pair of axes with their spectra beside them in Figure 5, the voltage scaled as $v_o/250$ so that the two traces share a scale. Table 6 collects the numbers: 187.7 V fundamental, 132.7 V rms, 2.53% voltage distortion and 0.23% current distortion, all inside the 5% ceiling of IEEE Std. 519-2022.

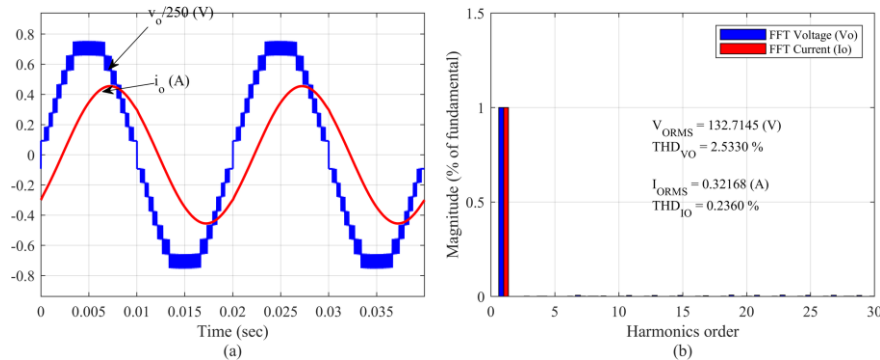


Figure 5: Simulated output voltage and load current with their FFT spectra under MASPWM control.

Table 6: Simulated performance of the proposed inverter under MASPWM control.

V_{fund} (V)	V_{rms} (V)	THD _V (%)	I_{rms} (A)	THD _I (%)
187.7	132.7	2.53	0.321	0.23

A distortion of 2.53% alongside a waveform with visibly separate steps deserves a check, and three independent ones are available. The first is an upper bound from quantisation. A staircase approximation with a step of size delta carries an error whose rms value cannot exceed delta divided by two root three, which for the 23.59 V step of this converter is 6.81 V, or 5.1% of the 132.7 V fundamental rms. The computed value lies below that bound, as it must, and the factor of two between them is what the nearest-level pattern produces, since its error follows the reference rather than being spread uniformly across the step. The second check is a determination by a different method altogether: the power-quality function of the oscilloscope returned 2.9% for the same quantity on the prototype, so a numerical result and an instrument measurement agree to within 0.4 percentage points. The third is the published range, since the seventeen-level converters collected in Table 10 report between 2.50% and 4.10%. The steps are visible because they are 23.59 V apart on a 187.7 V peak; seventeen of them follow the reference closely enough that what is left over is a few per cent, which is the reason the converter needs no output filter.

The four capacitor voltages settle within a few cycles of start-up and stay there: C1 and C2 hold about 47.83 V and 46.81 V, C3 and C4 about 23.68 V and 22.69 V, which is the asymmetric split the design asked for, and Figure 6 records the whole interval. The ripples run 2.5%, 4.3%, 8.4% and 8.6%, all under the 10% limit that set the capacitance in section 2.6. Nothing balances them; no measurement is taken and no correction applied at any point in the cycle.

The blocking voltages divide the fourteen devices into three groups and the currents into two, with every peak gathered in Table 7 and the complete records given in Figures 7 and 8. S1, S2, S5 and S6, which reverse the polarity, block 143.3 V, about three quarters of the peak output. S4 blocks 96.0 V, S3, S13 and S14 block 48.0 V, S7 to S10 and S12 about 47.4 V, and S11, which only touches the divider midpoint, blocks 23.4 V. The total standing voltage is 1073.6 V and no device ever sees the full output. That grading is worth money: only four positions need devices rated above 100 V, the rest can use cheaper 100 V parts with lower on-state resistance. On the current side the load-path switches stay below 2.1 A while

S14 takes the short charging spikes near 12 A that the inductor of section 2.6 holds down.

Table 7: Simulated peak and RMS voltage and current stress of the power switches.

Switch	Peak voltage (V)	Peak current (A)	RMS current (A)
S1	143.3	0.46	0.249
S2	143.3	0.46	0.212
S3	48.0	0.47	0.285
S4	96.0	2.10	0.466
S5	143.3	1.77	0.426
S6	143.3	1.75	0.459
S7	47.4	1.77	0.444
S8	47.4	1.75	0.441
S9	47.4	0.46	0.148
S10	47.4	0.46	0.193
S11	23.4	0.46	0.217
S12	47.4	0.46	0.283
S13	48.0	0.47	0.221
S14	48.0	11.93	0.929
TSV	1073.6 V	—	—

Four panels have been drawn out of Figures 7 and 8 and gathered in Figure 9, because the grids show the pattern while the detail is what a designer selects devices from. S5 blocks the most, 143.3 V, which is 0.76 of the peak output and 3.04 times the input, because it stands across the full series string at the extreme levels. S11 blocks the least, 23.4 V, exactly half the input, because it only ever connects the midpoint of the capacitor divider and so sees a single half-step. The four-to-one spread between them is the practical dividend of the asymmetric arrangement: four of the fourteen positions need devices rated above 100 V and the remaining ten can take cheaper 100 V parts with lower on-state resistance, which is why the conduction loss of section 5.3 comes to only 0.62 W for a converter of this level count.

The two current panels make a different point. S4 carries 2.10 A at the peak, the largest of the load-path devices, because it conducts the series string at the high levels, and its waveform follows the load current directly. S14 carries 11.93 A at the peak, but that is not load current at all: it is the capacitor charging pulse held down by the soft-charging inductor, and its rms value is 0.929 A. A ratio of nearly thirteen to one between peak and rms is what lets a modest device serve in the charging path in spite of the peak, and it is also why the inductor is there, since the same pulse would otherwise reach the 175 A that the path resistance alone would allow.

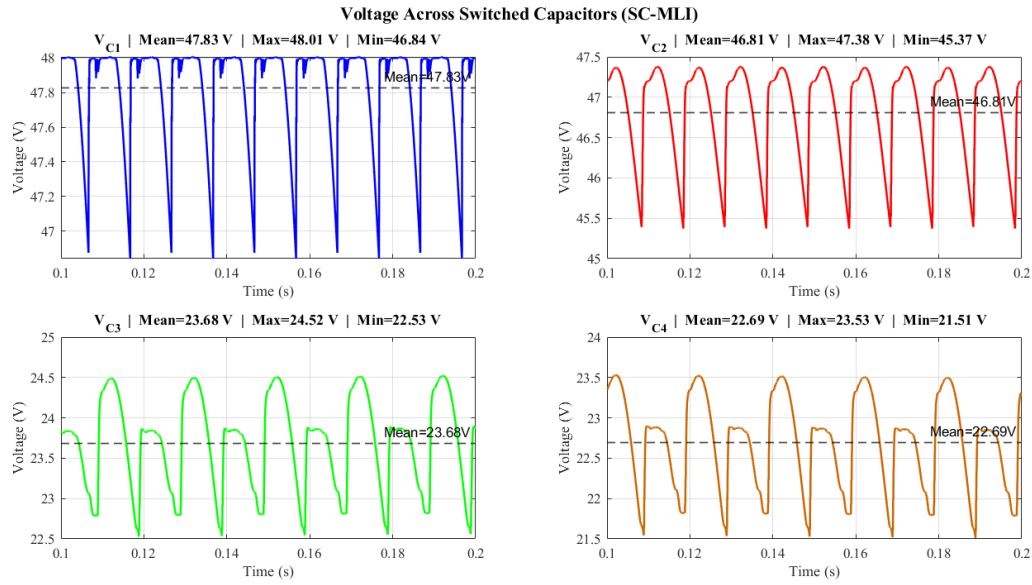


Figure 6: Simulated switched-capacitor voltages VC1 to VC4 confirming self-balancing.

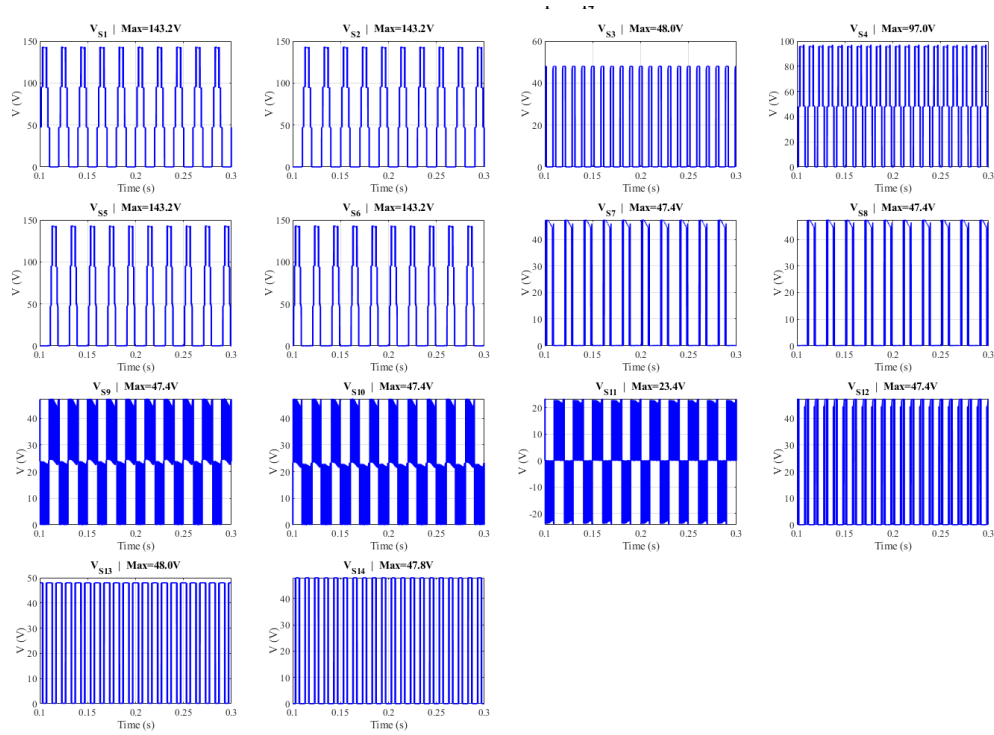


Figure 7: Voltage stress across the power switches S1 to S14.

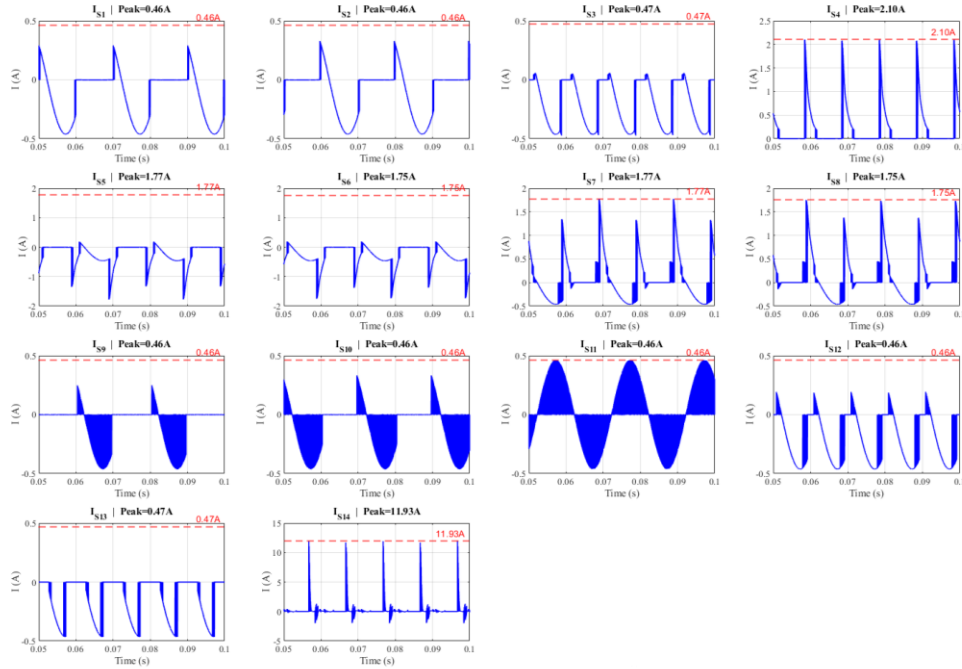


Figure 8: Current stress across the power switches S1 to S14.

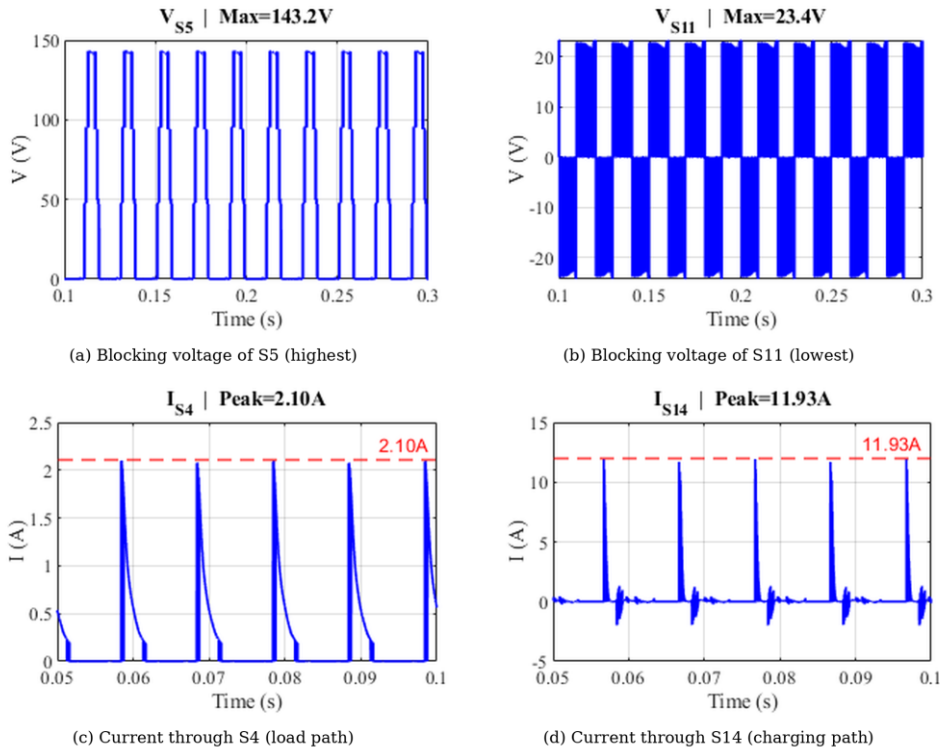


Figure 9: Representative device stress waveforms drawn from Figures 7 and 8: (a) blocking voltage of S5, the most stressed device; (b) blocking voltage of S11, the least stressed device; (c) current through S4, the most stressed device in the load path; (d) current through S14, a charging-path device.

5.2 Experimental Results

With the motor connected and $M_a = 1$ the prototype reproduces the simulated waveform closely. Eight steps of about 23.6 V build each half-cycle, the peak reads 186.7 V against a theoretical 188.7 V, a gain of 3.96, and the fundamental rms is 132.3 V where the model predicted 132.7 V. This is a non-unity power factor test throughout: the machine draws a lagging current at a power factor of 0.76, so the converter supplies reactive power in every measurement reported here, and the staircase holds its shape regardless. The measured records are collected in Figure 10.

The distortion of the output current was measured under the same conditions as the voltage and comes to 2.8%, against 2.9% for the voltage. Both were read from the power-quality function of the instrument on the running prototype, and both sit close to the 2.53% the model predicted for the voltage, which says that the machine draws a current whose shape is set by the quality of the applied voltage rather than by any deficiency of the converter. The simulated current distortion of 0.23% is a different quantity and should not be read as a discrepancy: the model represents the motor as an ideal series resistance and inductance, a linear filter that removes almost all of the stepped content, whereas the measured current flows in a real machine whose magnetising branch saturates over the cycle, whose auxiliary winding is closed through an 8-microfarad run capacitor and whose slotting contributes harmonics of its own. The measured 2.8% therefore carries contributions from the load that the model does not contain, and it is the figure to quote for this converter driving this machine.

On the bench the capacitors settle exactly where the analysis put them: C1 and C2 hold 47.99 V and 46.57 V against a nominal 47.175 V, C3 and C4 hold 22.94 V and 22.69 V against 23.59 V, and the ripples run between 2.3% and 4.5%, as listed in Table 8. The hardware balances itself exactly as section 2.5 said it would, and every ripple stays inside the design limit. Simulation and measurement are set against each other in Table 9. On the voltage side the gaps are small and all point the same way: 1.0 V less fundamental, 0.4 V less rms, 0.4 points more distortion and 94.6% efficiency instead of 96.5%, which device drops, the 2-microsecond dead time and a motor that is not the ideal inductance of the model account for between them. On the current side the gap is larger and has a different cause, discussed above: the ideal series R-L of the model filters the staircase almost perfectly, while the machine on the bench does

not. Nothing in the comparison points to a mechanism in the converter that the analysis missed.

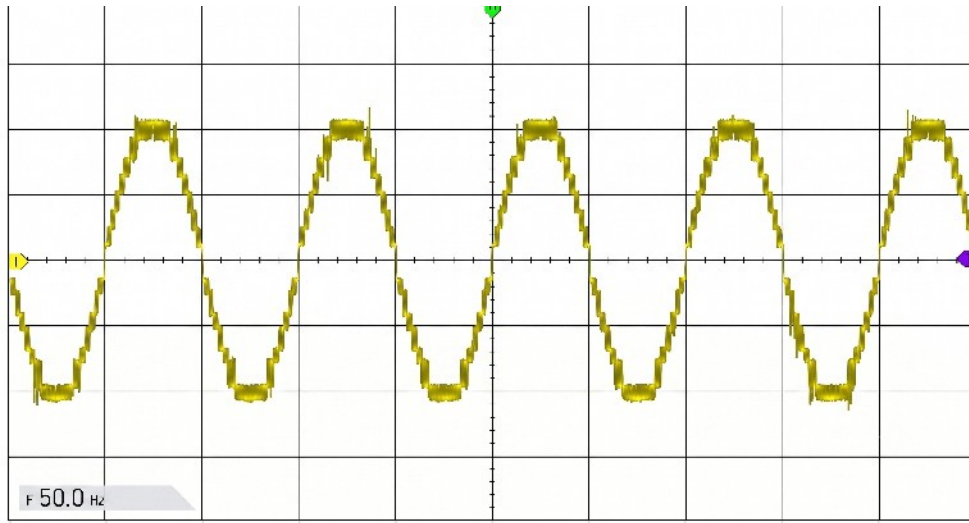
5.3 Where the losses go

The efficiency figure is only useful if one can say what makes up the missing 5.4%. At the rated point the converter delivers 32.9 W at 94.6%, so 1.88 W is dissipated, and that budget can be built term by term from quantities the paper has already reported. Table 11 collects the result.

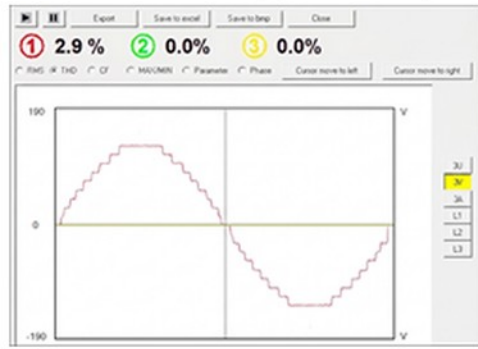
Conduction comes first and is the only term that can be computed exactly: summing I_{rms}^2 times R_{on} over the fourteen switches, with the rms currents of Table 7 and $R_{on} = 0.27$ ohm, gives 0.62 W, a third of the total. Switching is the smallest term. Under MASPWM each device turns on and off once per cycle, so the converter performs 1400 commutations per second in total; even at 50 microjoules per commutation, a generous bound for a 500 V device operating at 48 V and a couple of amperes, that is 0.07 W. A 10 kHz carrier scheme would multiply this term by two hundred, which is the quantitative form of the argument made in section 3.1.

The capacitor charging term is the interesting one. Charging a capacitor through a resistance dissipates half C times ΔV^2 squared per event regardless of the resistance value; with the measured ripples of Table 8 and two charging events per cycle this hard-charging bound comes to 2.31 W, which is more than the entire measured loss. The converter therefore cannot be charging its capacitors resistively, and the difference is the work done by the soft-charging inductor: the residual of the budget puts the actual charging loss near 1.09 W, roughly 47% of the bound. This is the clearest evidence in the paper that the branch of section 2.6 does what it was designed to do, and it is obtained without any additional measurement.

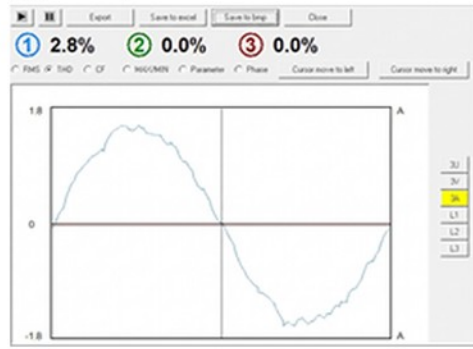
Scaling matters as much as the present split. Conduction and capacitor charging both grow with the square of the load current, the inductor copper loss likewise, while the switching term grows roughly linearly. At twice the tested current the first two terms would rise to about 2.5 W and 4.4 W against an output of 66 W, so the efficiency would fall to roughly 90% unless the on-state resistance and the capacitance were scaled with the power. That is the design rule this budget yields: at higher power the converter is dominated by conduction and charging, not by switching, so lower R_{on} devices and larger capacitors buy more than faster ones.



(a) Measured output voltage, 50 V/div, 10 ms/div



(b) Measured voltage THD = 2.9 %



(c) Measured current THD = 2.8 %

Figure 10: Measured performance of the prototype feeding the 180 W single-phase induction motor: (a) output voltage at 50 V/div and 10 ms/div; (b) measured output-voltage harmonic distortion, 2.9%; (c) measured output-current harmonic distortion, 2.8%.

Table 8: Measured switched-capacitor voltages and ripples.

Capacitor	Nominal (V)	Mean (V)	Max (V)	Min (V)	Ripple (V)	Ripple (%)
C1	47.18	47.99	48.60	47.40	1.20	2.5
C2	47.18	46.57	47.04	45.99	1.05	2.3
C3	23.59	22.94	23.43	22.41	1.02	4.4
C4	23.59	22.69	23.18	22.16	1.02	4.5

Table 11: Measured loss budget of the prototype at the rated operating point.

Loss mechanism	Value (W)	Share	How it was obtained
Switch conduction	0.62	33 %	sum of $I_{rms}^2 R_{on}$ over the fourteen switches, $R_{on} = 0.27 \Omega$
Capacitor charging	1.09	58 %	residual of the budget; hard-charging bound is 2.31 W
Soft-charging inductor	0.09	5 %	$I_{rms}^2 R_{dc}$ with $I_{rms} = 0.93$ A, $R_{dc} = 0.1 \Omega$
Freewheeling diode D_r	0.03	2 %	$V_F = 1.2$ V over the freewheeling interval
Switching	0.07	4 %	upper bound: 1400 commutations/s at 50 μ J each
Total	1.88	100 %	measured efficiency 94.6 % at 32.9 W output

5.4 Behaviour under load and input variation

MASPWM fixes its angles once the level count is chosen, so the obvious question is what happens when the operating point moves. Three cases matter, and each has a different answer.

Input voltage first. The converter is an open-loop multiplier: the peak output is $4V_{in}$ whatever V_{in} happens to be, so a ten per cent change in the source produces a ten per cent change in the output and nothing else. The capacitor voltages track the source in the same proportion, $V_{C1} = V_{C2} = V_{in}$ and $V_{C3} = V_{C4} = 0.5V_{in}$, so the ratios that the balancing argument of section 2.5 depends on are untouched; the converter neither loses levels nor loses balance. Where output regulation is required, it has to come from the DC side, either from a regulated bus or from the carrier-based mode that the same FPGA already carries.

Load fluctuation second. The load current does not appear anywhere in the switching table, so the level structure is unaffected by it; what changes is the ripple, and it changes proportionally, because the charge removed during a discharge interval is $Q = I_0 \cdot t_{MDD}$. Doubling the load current from the tested 0.46 A to 0.92 A therefore doubles the ripple of C1 from 2.5% to about 5%, and that of C3 from 4.4% to about 8.8%, both still inside the 10% design limit. The margin of twelve built into the capacitor sizing in section 2.6 is what buys this headroom; at four times the tested current the divider capacitors would exceed the limit and would have to be increased.

Sudden load steps third, which is the transient question. The recovery is set by the resistive charging path rather than by any controller: from the derivation of section 2.5 the deviation of a capacitor voltage decays with the time constant $R_{on} \cdot C$, here 0.27-ohm times 10 mF, that is 2.7 ms. Five-time constants, 13.5 ms, is about two thirds of a fundamental period, so a step-in load current is absorbed within roughly one cycle and the capacitors return to their nominal values in the next. This figure is analytical, derived from the same model as the balancing proof, and it agrees with the observation reported in section 5.2 that the output waveform recovers its multilevel structure within one cycle of a modulation-index step. A direct oscilloscope record of a load step, with the ripple envelope and the recovery captured simultaneously, was not possible with a two-channel instrument and one current probe, and is listed among the future work.

Table 9: Simulated and measured performance under MASPWM control.

Metric	Simulation	Experiment
V_{fund} (V)	187.7	186.7
V_{rms} (V)	132.7	132.3
THD _v (%)	2.53	2.9
THD _i (%)	0.23	2.8
Voltage gain	4.00	3.96
V_{C1} / V_{C2} (V)	47.83 / 46.81	47.99 / 46.57
V_{C3} / V_{C4} (V)	23.68 / 22.69	22.94 / 22.69
Efficiency (%)	96.5	94.6

5.5 Comparison with Existing Topologies

Table 10 sets the converter beside the seventeen-level switched-capacitor inverters it should be judged against. The counts are reproduced as the original authors state them, and only designs whose counts could be confirmed from the source papers are listed. Total standing voltage is the sum of the peak blocking voltages of all switches, and the cost function of (17) normalises the component effort per output level.

$$CF = (N_{SW} + N_{GD} + N_D + N_C + \gamma \cdot PIV_{pu} + \alpha \cdot TSV_{pu}) \cdot N_{DC} / N_L \quad (17)$$

In (17) NSW, NGD, ND, NC and NDC count the switches, gate drivers, diodes, capacitors and DC sources, NL is the number of levels, PIV_{pu} and TSV_{pu} are the per-unit peak inverse and total standing voltages referred to the peak output, and gamma and alpha weight the two of them, both set to one here. For this converter, with NSW = NGD = 14, ND = 2, NC = 4, NDC = 1, NL = 17, PIV_{pu} = 0.76 and TSV_{pu} = 5.69, the cost function comes to 2.38. The comparison should be read honestly. On component count the proposed converter is the largest of the group: twenty main power components against sixteen for Sun et al. (2022) and Haghghian et al. (2023), seventeen for Mansourizadeh et al. (2025) and nineteen for Dhanamjayulu et al. (2021) and Chandan et al. (2024). Its component-to-level ratio, CLR = (NSW + NC + ND)/NL = 20/17 = 1.18, is correspondingly the highest. No claim of a component-count advantage is made here, and the fourfold gain does not buy one back: Mansourizadeh et al. reach the same gain with seventeen components and Chandan et al. reach eight times the input with nineteen.

What the extra components buy is where the argument lies. The blocking voltages are graded over a four-to-one range, with a total standing voltage of 1073.6 V, 5.69 per unit, and a peak inverse voltage of

0.76 per unit, so ten of the fourteen positions can take low-voltage devices; the cost function of (17) evaluates to 2.38 for this converter, and we report it for this converter only, since the per-unit blocking voltages of the others are not published and no claim is made about their values. More to the point, every converter in Table 10 is driven by a carrier-based scheme that commutates its devices at kilohertz rates,

whereas the converter reported here runs at the fundamental frequency from eight precomputed angles. That is what holds the switching loss to 0.07 W of the 1.88 W measured total, and it is the trade the design actually makes: a few more devices, each switching a hundred times less often.

Table 10: Component comparison with reported 17-level switched-capacitor inverters, where $Total = N_{sw} + N_c + N_d$ and $CLR = Total/N_L$. Counts are as stated by the original authors; n.r. = not reported separately. *Haghighian et al. derive two DC links from a flyback front end whose components are not included in their total.

Reference	Levels	N_{sw}	N_c	N_d	N_{dc}	Total	CLR
Sun et al. (2022)	17	10	4	2	1	16	0.94
Haghighian et al. (2023)	17	10	n.r.	n.r.	2*	16	0.94
Dhanamjayulu et al. (2021)	17	13	4	2	1	19	1.12
Chandan et al. (2024)	17	13	3	3	1	19	1.12
Mansourizadeh et al. (2025)	17	10	4	3	1	17	1.00
Proposed converter	17	14	4	2	1	20	1.18

5.6 Trade-offs, Applications and Limitations

The design has its costs, and the largest of them is the part count. Fourteen switches are more than the ten to thirteen used by the seventeen-level converters of Table 10, and each one wants a driver. MASPWM buys much of that back by commutating everything at 50 Hz, and the graded blocking voltages mean most positions take cheap 100 V devices. What MASPWM cannot give is amplitude control: the angles are fixed by construction, so anything needing output regulation has to act on the DC link.

Scaling up is a matter of ratings rather than structure. Three identical modules on one source make a three-phase system, and higher power means re-rating the switches and the soft-charging inductor, whose peak currents follow the load current. The MDD sizing of section 2.6 scales linearly with I_0 , so it survives the move. Together with the fourfold boost that puts the converter in reach of PV string inverters, battery-fed auxiliary drives and small single-phase motors of the kind tested here, where dropping the front-end DC-DC stage saves both efficiency and cost.

Three limits deserve saying out loud. The measurements come from one single-phase prototype at low power with one motor, so higher power and three-phase operation remain unproven. The inrush limiting was checked in simulation only, because the current probe available could not capture the start-up transient cleanly. And while the motor load used throughout is a non-unity power factor load, at 0.76 lagging, a recorded transient of a sudden load step

was beyond a two-channel instrument with a single current probe; the response time given in section 5.4 is therefore analytical, not measured.

6 CONCLUSIONS

A seventeen-level switched-capacitor inverter with unequal capacitor voltages was designed, analysed and measured under MASPWM control. The power stage turns one DC source into seventeen levels and four times the input voltage using fourteen switches, four capacitors and two diodes, and MASPWM drives it from eight precomputed angles, so every device switches once per half-cycle and the zero level never appears.

Balancing was proven by charge conservation and by a Lyapunov argument, then confirmed on the bench with capacitor ripples of at most 4.5% and no correcting action anywhere. Simulation gives 187.7 V with 2.53% voltage distortion and 0.23% current distortion; the prototype gives 186.7 V, a measured voltage distortion of 2.9% and a measured current distortion of 2.8% with no output filter, a gain of 3.96 and about 94.6% efficiency, all within IEEE Std. 519-2022. The total standing voltage is 1073.6 V, that is 5.69 per unit, and the cost function of the proposed converter is 2.38; the per-unit blocking voltages needed to compute the same figure for the compared designs are not published, so no ranking is claimed on that metric. On component count the converter uses twenty main power components for its seventeen levels, a component-to-level ratio of 1.18, which is higher than the seventeen-level designs it is compared

with; the case for it rests not on part count but on reaching a fourfold gain and a filterless 2.9% distortion while every device commutates only twice per cycle.

The work stops at a single-phase prototype driving one motor, with the start-up current limiting shown only in simulation and with no way to vary the modulation index under MASPWM. Next comes a three-phase version at higher power, a proper measurement of the start-up transient, and closed-loop grid-connected control, for which the carrier-based modulation already sitting on the same FPGA supplies the amplitude freedom that MASPWM does not.

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