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Analysis and Simulation of Charge Pump Circuits Under the Influence of Parasitic Capacitance

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Abstract:

Charge pump circuits is a type of DC-DC converter in which different DC level can be obtained from constant DC input level. Usually, CP circuit are designed to be realized as integrated circuit form. One of the most important factors that affect the operation of analog IC is the parasitic capacitance associated with transistors and capacitors where it is effect is at high frequencies on the output voltage as well as the efficiency because it drains a portion of the charge being transferred and thus negatively affects the performance of the electronic circuits. This paper presents a comparative study between four different CP realizations in terms of its sensitivity to parasitic capacitances associated with pumping capacitors and note which of these topologies is more affected by parasitic capacitors since the aim of CP implementation is the integrated realization of these circuits. This paper includes a comparison between mathematical analysis and simulation using Advanced Design System (ADS) simulation software to evaluate the performance of these circuits.

Keywords: *Charge pumps, Dickson CP, Cockcroft-Walton CP, Pelliconi CP, Bootstrap CP.*

1 INTRODUCTION

The role of Charge pump circuits is to provide output voltages several times higher than the regular supply voltage depending on the number of stages used the Figure(1) shows a block diagram of a charge pump. Given the low voltage present in the power supply of integrated circuits (ICs), charge pump play an important role in raising this voltage without using inductors, which makes these charge pump suitable for integrated circuits due to their limited area. The most essential applications CP may contain nonvolatile storage, such as EEPROM or flash memory, to write or erase the floating-gate devices. A charge pump is used in flash memory to create the high voltages required for erase and write operations(Jinbo *et al.*, 1992)(Palumbo, Pappalardo and Gaibotti, 2006). CPs are originally used in smart power ICs. The Dickson CP circuit was proposed by John F. Dickson in 1976 . It works in a similar manner to the Cockcroft-Walton CP circuit. However, the boost capacitors in the Dickson CP are connected in parallel instead of in series in the Cockcroft-Walton CP and one plate of the capacitors is always connected to the intervening clock signal. The major benefit of diodes is the elimination of switch control signals. The biggest drawback is the lower output voltage of the CP. In fact, when the diode is forward biassed (i.e., when the accompanying switch is closed), it produces a voltage loss equal to the diode's threshold value, VD, lowering the working output voltage, VD(N+1). This drop is particularly substantial under low power supply, resulting in a loss of efficiency(Tanzawa and Tanaka, 1997)(Weiner, 1969). The Dickson and Cockcroft-Walton charge pump mentioned above suffer from the drawback of losing efficiency due to the threshold voltage and body effect. The four-phase Bootstrap charge pump(Umezawa *et al.*, 1992) is a solution to eliminate the threshold voltage and body effect by using an NMOS switch to reduce the threshold voltage effect that affects the output voltage and output resistance(Bi, 2023). Pelliconi suggested another form of charge pump that is distinct from the Dickson charge pump and is straightforward to execute(Pelliconi *et al.*, 2001). This charge pump concept uses control signals to turn on and off the MOS switches. The two-phase non-overlapping clock signals Vclka and Vclkb serve as both control signals for the MOS switches and the DC power supply, which transfers charge from stage to stage. In this

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circuit, PMOS and NMOS switches are used to reduce the effect of the threshold voltage that affects the output voltage and output resistance. The Cockcroft-Walton

(Cockcroft and Walton, 1932), diodes and capacitors are employed to generate a higher voltage. A series of diodes are connected to the inputs via series capacitors; therefore, the Cockcroft charge pump is sensitive to parasitic capacitors more than others. Parasitic capacitors do not contribute to the useful operation of the circuit, but they do affect the output voltage and output resistance(Dickson, 1976). The fourth structure considered in this paper of CP is the Bootstrap charge pump that eliminates the threshold voltage drops in MOS by increasing the NMOS's gate to source voltage. Therefore, transferring the charge to the remaining stages is easy, as the Bootstrap charge pump (Atsumi *et al.*, 1994)(Palumbo and Pappalardo, 2010). The realization contains an additional MOS device and Bootstrap Capacitor Cbt for each stage compared to the Dickson charge pump. It is also suffered from parasitic capacitance the effect the output voltage and output resistance. This paper a comparative study between the four topologies mentioned above in terms, of their complexity, and their sensitivities to the effect of parasitic capacitances.

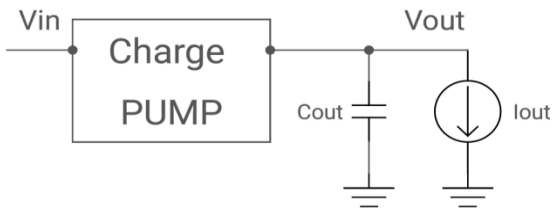

Fig.1 . Charge pump block diagram.

CP was proposed by John Douglas Cockcroft and Ernest Thomas Sinton Walton

2 PARASITIC CAPACITORS

Analoge integrated circuits including integrated charge pump circuits are affected by parasitic capacitors. Transistor parasitic capacitance from each node to substrate have negligible effect compared with that parasitic in IC capacitors (Ker, Chen and Tsai, 2006)(Toft and Jorgensen, 2021). The parasitic capacitance associated with each node from bottom and top plate electrons in the fabricated IC capacitor. The typical values of parasitic capacitances in analog MOS integrated circuits are (1% to 5%) of actual value for the top plate and (1.5% to 20%) for the bottom plate from the pumping capacitor (Allasasmeh and Gregori, 2010)(Allasasmeh and Gregori, 2010). The output voltage of CP and output resistance influenced by parasitic capacitors associated(Ho *et al.*, 2022). Some techniques can be used to reduce the effect of parasitic capacitors on charge pumps, including reducing the frequency because it reduces the charging and discharging rates, as well as using capacitors with low parasitic capacitance. Figures (2), (3), (4), and (5) presents the four CP realization under study including parasitic capacitors. Table(1) and Table(2) summarized the mathematical formulation of the parasitic effect on these four structures on output voltage and output resistance (Pelliconi *et al.*, 2001)(Dickson, 1976)(Pulvirenti, 2022).

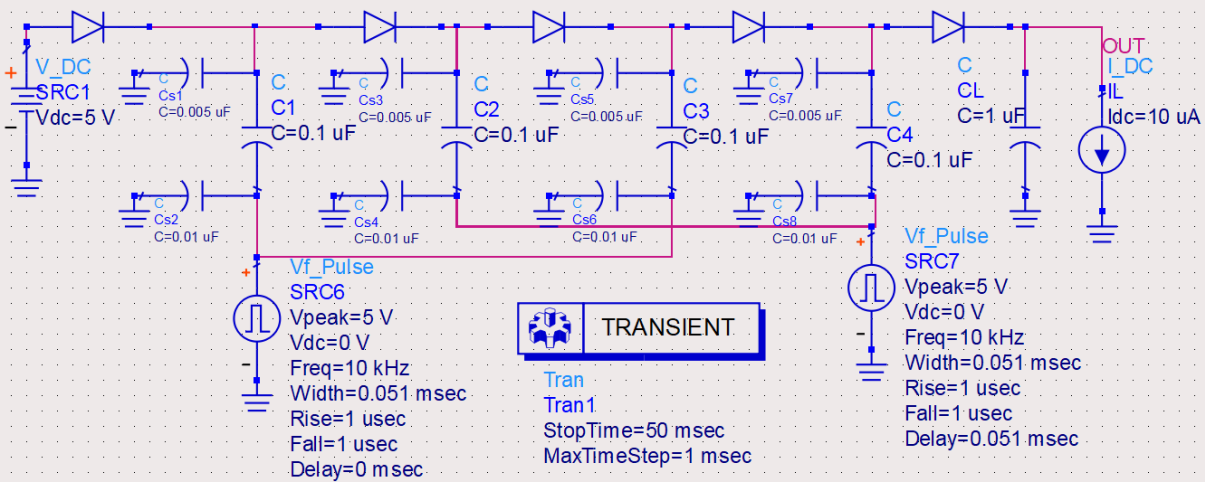

Fig. 2. Dickson charge pump with parasitic capacitors.

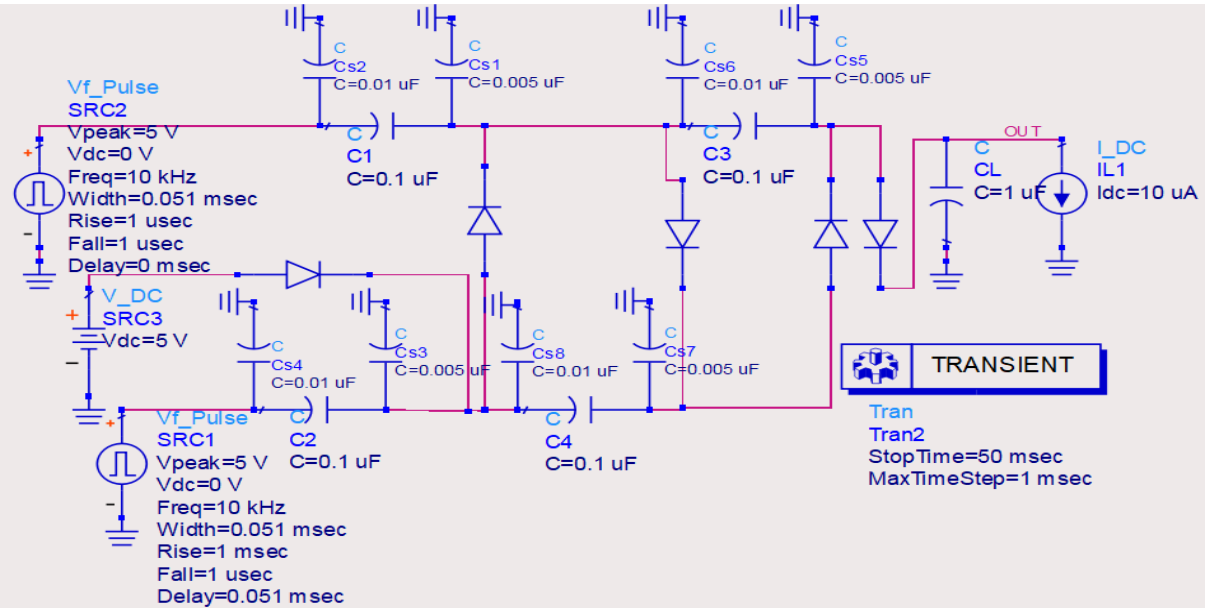

Fig. 3. Cockcroft-Walton charge pump with parasitic capacitors.

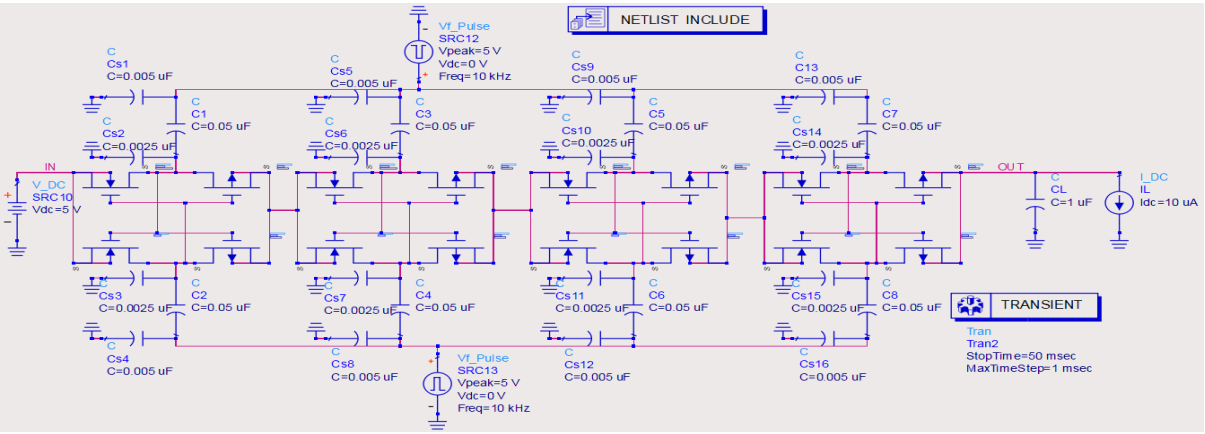

Fig. 4. Pelliconi charge pump with parasitic capacitors.

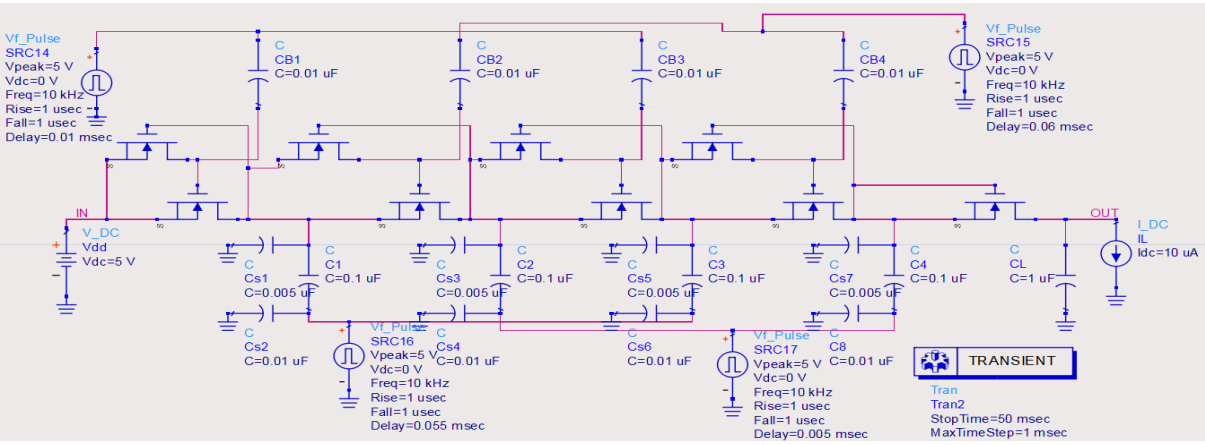

Fig. 5. Bootstrap charge pump with parasitic capacitors.

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Table 1: Output voltage and output resistance without parasitic

Topology	Vout without parasitic	Rout without parasitic
Cockcroft-Walton	Vo= VIN − (N + 1) VD + NVCK – Io*Ro	Ro= $\frac{1}{f.\,cp}.2\sum_{i=1}^{\frac{N}{2}} i^2$ N even Ro= $\frac{1}{f.\,cp}.[\sum_{i=1}^{\frac{N+1}{2}} i^2 + \sum_{i=1}^{\frac{N-1}{2}} i^2\ ]$ N odd
Dickson	Vo= (N+1).(VDD – Vth) - $\frac{N.Io}{f.cp}$	Ro= $\frac{N}{f.\,cp}$
Pelliconi	Vo= VIN + N(Vclk - $\frac{Io}{2*cp.f}$)	Ro= $\frac{N}{2*f.\,cp}$
Bootstrap	Vo= VIN + N(Vclk - $\frac{Io}{cp.f}$)	Ro = $\frac{N}{f.\,cp}$

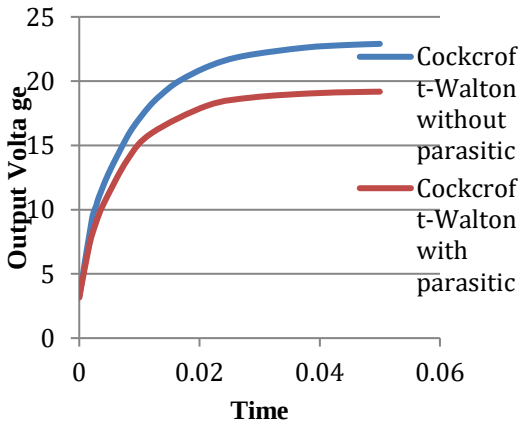
Table 2: Output voltage and output resistance with parasitic.

Topology	Vout with parasitic	Rout with parasitic
Cockcroft-Walton	Vo= VIN −(N + 1) VD+2$\sum_{i=1}^{\frac{N}{2}} \prod_{j=1}^{i} \frac{1}{1+\alpha SV(j)}$ Vck - Io*Ro N even Vo= VIN − (N + 1) V D + [$\sum_{i=1}^{\frac{N+1}{2}} \prod_{j=1}^{i} \frac{1}{1+\alpha SV(j)} + \sum_{i=1}^{\frac{N-1}{2}} \prod_{j=1}^{i} \frac{1}{1+\alpha SV(j)}$] .Vck - Io*Ro N odd	Ro= $\frac{1}{f.\,cp}$. $2\sum_{i=1}^{\frac{N}{2}} \sum_{j=1}^{i} \frac{N-j+1}{1+\alpha SR(j)}$]. Vck N even Ro= $\frac{1}{f.\,cp}$ [$\sum_{i=1}^{\frac{N+1}{2}} \sum_{j=1}^{i} \frac{N-j+1}{1+\alpha SR(j)}$ + $\sum_{i=1}^{\frac{N-1}{2}} \sum_{j=1}^{i} \frac{N-j+1}{1+\alpha SV(j)}$] N odd
Dickson	Vo=VDD+N($\frac{cp}{cp+cs}$).Vclk –Vth - $\frac{Io}{fclk(cp+cs)}$) - Vth	Ro= $\frac{N}{f(cp+cs)}$
Pelliconi	Vo=VDD+N($\frac{cp}{cp+cs}$).Vclk – $\frac{Io}{2*fclk(cp+cs)}$)	Ro= $\frac{N}{2*f(cp+cs)}$
Bootstrap	Vo=VDD+N($\frac{cp}{cp+cs}$).Vclk – $\frac{Io}{fclk(cp+cs)}$)	Ro= $\frac{N}{f(cp+cs)}$

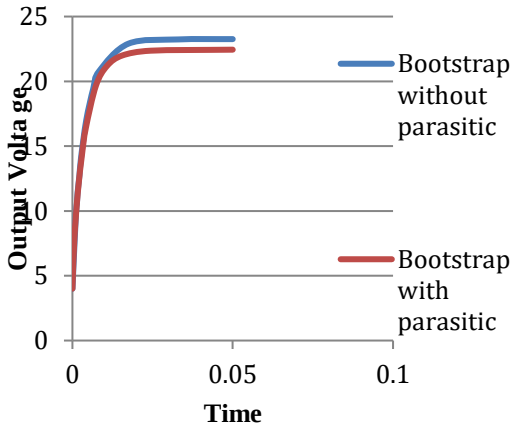
3 Design and simulation results

An analytical and simulation procedures and employed for the comparison purposes, and a comparative study using Advanced Design System(ADS) for the four structures under consideration. The design of four stage CP circuits is considered with input voltage of 5Volt and a selected load current of 10μA using frequency of 10KHZ and using a stage capacitor of 0.1μF as a case study. The Dickson charge pump is designed using a 1N4148 diode, the Cockcroft-Walton charge pump is designed using a 1N4148 diode, the Pelliconi charge pump is designed using a PMOS and NMOS transistors and the Bootstrap charge pump is designed using an NMOS_2SK579 transistor. First, a comparison is employed for each type separately with the presence of parasitic capacitors and with the absence of parasitic capacitors. The effect of parasitic capacitors for the four stages are calculated and simulated by selecting a typical value of 0.05 for the top plate capacitors and 0.1 for the bottom plate capacitors from the stage capacitor where the top plate capacitor can be expressed βC and the bottom plate capacitor as αC. It is found the bottom plate capacitor has no effect because it is connected to ideal source (Toft and Jorgensen, 2021). It is noticed that the effect of the parasitic capacitors on the Cockcroft-Walton charge pump is greater than the others because the stage capacitors of this charge pump are connected in series, and for this reason, it is also noticed that the effect on the output voltage is large.

Table(3) presents a comparison between the output voltages for the four structures in terms of their sensitive to parasitic capacitors(Song and Ikehashi, 2024), and also compared with that without parasitic capacitors. The comparison include mathematical and ADS simulation results. It is found that Pelliconi has lowest voltage variation ΔV because the effect of parasitic capacitors on it is small and the reason is that the stage capacitor of this structure is divided by two, and the worst structure the influenced by parasitic capacitor is Cockcroft-Walton. Table(4) illustrate the effect of parasitic capacitors on the output resistance of these topologies, analytically and simulation. The Table(5) represents a comparison between this work and other works that were previously conducted(Abaravicius, Cochran and Mitra, 2021)(Shen, Bose and Johnston, 2018)(Navidi and Graham, 2017). The Table(6) shows a mathematical comparison between the results of this work and other works conducted previously(Hsu and Lin, 2010). The simulated output resistances and obtained from the transient responses shown in Figure(6)(a,b,c,d) by determining the time constant that govern those transient responses. It can be seen from these result that the parasitic capacitances have a small effect on the output resistances. Figure(7)(a,b) presents a transient response of output voltages for the considered topologies under the effect of parasitic capacitances. It is clear from this figure that Cockcroft-Walton structure is move sensitive to parasitic capacitance compared with the other realizations.



a) Presents the transient response for Cockcroft-Walton CP.



b) Presents the transient response for Bootstrap CP.

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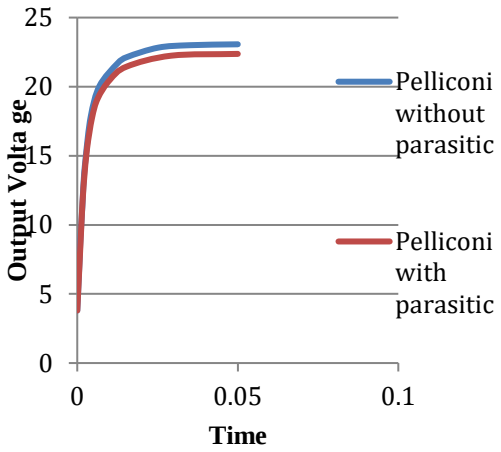
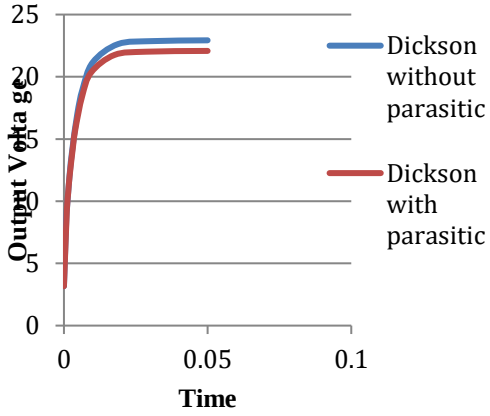
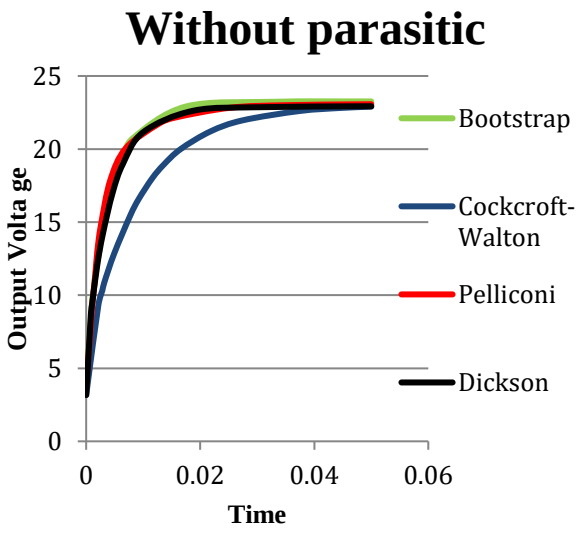


c) Presents the transient response for Pelliconi CP.

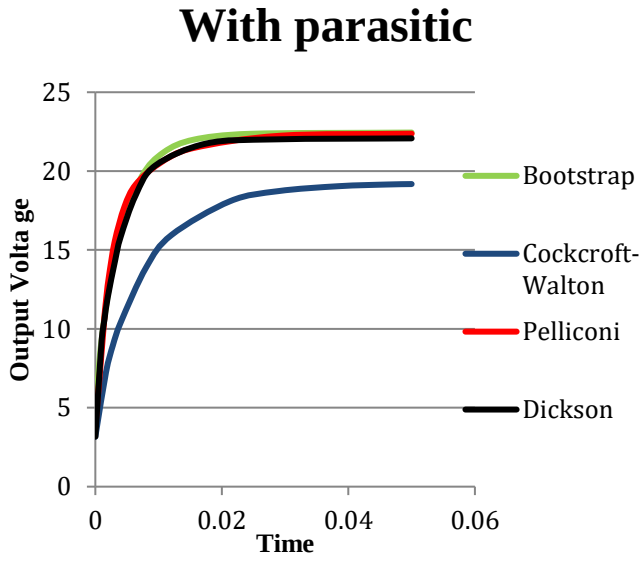


d) Presents the transient response for Dickson CP.

Fig. 6. Presents the transient response ADS simulated for the four structures with and without capacitors individually.



a) Present these structures without parasitic capacitors.



b) Present these structures with parasitic capacitors.

Fig. 7. Present the comparison for these structures with the existence of parasitic capacitors that illustrate the behavior of each type under the effect of parasitic.

Table 3: Output voltage of four charge pumps with parasitic capacitors and without parasitic capacitors

Topology	**Vout Without Parasitic calculated**	**Vout With Parasitic calculated**	**ΔV**	**Vout Without Parasitic simulation**	**Vout With Parasitic simulation**	**ΔV**
Dickson	23.11V	22.16V	0.95V	22.9V	22.076V	0.824V
Pelliconi	24.96V	24V	0.96V	23V	22.371V	0.629V
Bootstrap	24.96V	24V	0.96V	23.258V	22.444V	0.814V
Cockcroft-Walton	23.05V	18.7V	4.35V	22.9V	19.18V	3.72V

Table 4: Output resistance of four charge pumps with parasitic capacitors and without parasitic capacitors.

Topology	**Rout Without Parasitic calculated**	**Rout Without Parasitic simulation**	**Rout With Parasitic calculated**	**Rout With Parasitic simulation**
Dickson	4KΩ	4.2KΩ	3.8KΩ	4.01KΩ
Pelliconi	4KΩ	4.034KΩ	3.8KΩ	4.15KΩ
Bootstrap	4KΩ	4.1KΩ	3.8KΩ	3.99KΩ
Cockcroft-Walton	10KΩ	9.14KΩ	9.52KΩ	8.19KΩ

Table 5: Comparison of the results of this work with the results of other works.

Parameters	**This Work**	**(Abaravicius, Cochran and Mitra, 2021)**	**(Shen, Bose and Johnston, 2018)**	**(Navidi and Graham, 2017)**
Supply Voltage(V)	5	3.1	3.3	2.5
Load current(μA)	10	60	150	25
Number of stages	4	4	11	6
Stage capacitor(F)	0.1μ	30p	1.2p	1.5p
Clock frequency(Hz)	10K	20M	50M	30M
Output Voltage(V)	25	26	19.6	16

Table 6: Comparison of the mathematical results of this work with the mathematical results of previous works.

Parameters	This work	(Hsu & Lin, 2010)
Voltage Supply(V)	5	1.8
Stage capacitor(F)	0.1μ	10p
Clock frequency(Hz)	10K	10M
Number of stages	4	4
Load current(A)	10μ	50μ
Output Voltage(V)	24	7.2

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4 CONCLUSIONS

Different topologies of CP circuits were investigated to study the effect of parasitic capacitors on their behavior. Dickson, Cockcroft -Walton, Bootstrap, and Pelliconi CP structures are designed and simulated. A four stage CP circuits are mathematically analysed with and without existence of parasitic capacitors. The effect of these parasitics is investigated to illustrate their influence on output voltage and output resistance. The comparison between these topologies shows in terms of the effect of the parasitic capacitors on each topology. It is noticed their effect on each topology and the reduction in the output voltage, it is effect on the Pelliconi charge pump is less because the stage capacitor is divided by two. but their effect on the Cockcroft-Walton topology is great because it suffers from parasitic capacitors more than others and also has a high output resistance because the capacitors are connected in series. The reason behind choosing these four topologies was to know which of these charge pumps is less affected by parasitic capacitors. Then it is made a comparison between mathematical and simulation results.

5 FUTURE WORKS

1. Design and optimization of charge pump circuits to reduce the effect of parasitics on them.
2. Study of the effect of clock frequency on parasitic capacitors.
3. Study of the effect of parasitics on the efficiency of charge pumps.
4. Carefully select charge pump circuits where parasitics will have little effect on them.
5. Optimizing chip area using genetic algorithm.

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Biography

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