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FPGA Based FIR Filter Structures for Radar Signal Processing

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Abstract

Digital filtering is one of the most efficient technologies for processing radar signals. FIR Filters are a very important type of Digital Filters that are a vital element in radar signal processing. Synoptic diagrams called "filter realization structures" show the connections between various arithmetical operations including add, multiplications, and shifts. Finite impulse response (FIR) filters can be realized using a variety of several types of structures or realizations such as direct form, cascade form, frequency-sampling form, and lattice structure. In this paper, FIR filter structures are proposed, simulated, and implemented using the Matlab Simulink Xilinx System generator blockset. These FIR Filter structures were developed using Xilinx System Generator (ISE Win 14.7) and Matlab Simulink (Win 2013). Xilinx System Generator tool provides a good way to design efficient hardware implementation for FIR filter structures on Artix-7 FPGA kit.

Keywords: *FIR filter structures, Digital filters, Xilinx System Generator, FPGA.*

1 Introduction

Filters have several uses in signal processing and communication systems, including financial data analysis, economic, biological signal processing, audio and video processing, and radar and noise reduction. To accomplish its filtering task, a digital filter processes digital input signals and generates other digital signals. Software and/or hardware are used to accomplish this mathematical approach (Madisetti 1999).

Because digital filters are such an important aspect of DSP, the need to implement them has arisen. A digital filter's impulse response may be divided into two categories: FIR (finite impulse response) and IIR (infinite impulse response) (Francis 2009). FIR filters are more complicated than IIR filters, but they also have several benefits that make them more popular in filtering applications. While FIR equivalents are always stable and are especially helpful for applications requiring accurate linear phase response, IIR filters do not give stability at higher orders (Anurag et al., 2013).

Synoptic diagrams called filter realization structures show the connections between different arithmetical operations including additions, multiplications, and shifts (Najim 2006). IIR and FIR filters each have a variety of structures.

(Gaikwad and Gawande 2014) suggested utilizing the Xilinx System Generator to design digital filters for audio applications. In addition, certain designs of digital filters utilizing the Xilinx System Generator and the MATLAB Simulink model are presented, and the outcomes of each are contrasted in terms of computing and storage needs.

(Das et al., 2016) showed FIR filter implementations using an FPGA kit. It is provided the Equiripple Method-based Low-Pass Higher Order FIR Filter. Utilizing the FDA Toolbox in MATLAB and the Xilinx System Generator, the coefficient and structure of this filter are computed. Low-pass filters are made to have stop band attenuation of 60 dB and sampling frequencies of 100 KHz, 10 KHz, and 20 KHz, respectively.

In order to produce high-order digital FIR filters with the least amount of hardware and logical delay, Jixi Li, et al. presented an enhanced distributed algorithm (DA) in (Bai et al., 2020). Look-up-table decomposition aids in the design and improvement of the parallel DA. The improved DA FIR filters are built using the Xilinx Kintex-7 FPGA package and used to process radar data in high-speed ground penetrating radar (GPR) systems. Examining and contrasting the efficiency of DA filters with varied ordering.

In this paper, different structures of FIR filter are presented and implemented using Artix-7 FPGA kit. The FIR filter structures are simulated with the help of Xilinx System Generator, while Xilinx ISE14.7 is utilized to estimate the hardware resources required.

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2 FIR Filter Structures

The system function of a FIR filter is of the following form:

$$H(z) = \sum_{n=0}^{M-1} b_n z^{-n} \qquad (1)$$

M is the filter's length and M − 1 is the filter's order. The structures of FIR filters are consistently stable. Structures in which the multiplier coefficients exactly match the system function coefficients are called direct form structure .The system function (1) is implemented directly in this way as stated. A cascade of second-order FIR sections can be used to create a higher-order FIR system function; this structure is referred to as a cascade form structure. The structure, which is based on the DFT of the impulse response h(n), is referred to as a frequency-sampling form structure and is ideal for a system design based on frequency response sampling $H(e^{jw})$. Lattice structure is the preferable structure type compared to other FIR filter structures because of its robustness and modularity, and has many applications in digital filtering (Ingle and Proakis C2010),(Bolic C2001).

3 Proposed FIR Filter

To construct any kind of digital frequency response, a FIR filter is utilized. The filter's output is produced using a sequence of delays, adders and multipliers. The delays in performing operations on earlier input samples. The coefficients used for multiplication, Filter design is the process of choosing the length and coefficients of the filter. The objective is to establish such settings so that the filter will operate with the specified stop band and pass band specifications. In order to create a multipurpose digital filter for radar signals using the FIR technique, the waveform of the transmitted radar signal is used to create the FIR filter According to (Ashwini and Venkataratnamm 2017). The suggested FIR filter's system function is provided in (2). **Figure 1** displays the 6th order FIR filter's frequency response.

$$H(z) = 0.08864 + 0.1381\,z^{-1} + 0.1752z^{-2} + 0.1889z^{-3} + 0.1752z^{-4} + 0.1381z^{-5} + 0.0886\,z^{-6} \qquad (2)$$

The FIR filter in (2) is realized using different FIR filter structures as shown in **Figure 2** and then implemented on FPGA Kit.

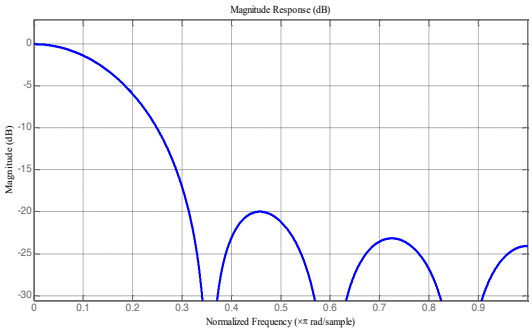

Figure 1: Frequency response for 6th order FIR filter.

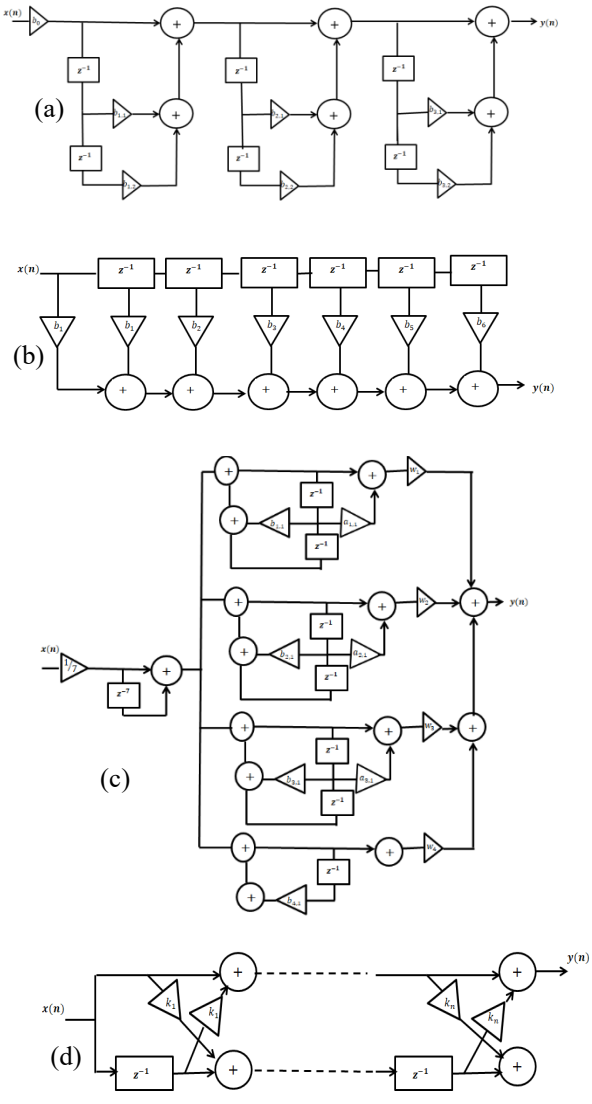

Figure 2: 6th order FIR filter structure (a) Direct Form structure (b) Cascade Form structure (c) Frequency-sampling Form structure (d) Lattice structure.

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4 FPGA Implementation

Utilizing the System Generator tool, the FIR filter Structures are implemented on the XC7A100T-1CSG324C Artix-7 FPGA Kit. For high-performance DSP systems built on FPGA, it is a high-level design tool (Xilinx, System generator for DSP). The accurate bit and cycle modelling of digital logic and DSP operations is made possible by the addition of software and blocks to Simulink (Moreo et al., 2004).

4.1 FIR Filter Structure with Direct Form Implementation

The system function H(z) in form (2) is implemented directly in this form as stated. The Direct form 6th order FIR filter structure displayed in **Figure 3**'s system generator model.

4.2 Implementation of Cascade FIR Filter Structure

The system function H(z) in (2) may be factored into three 2nd-order pieces, which can then be implemented using a cascade, as shown in (3). **Figure 4** shows Cascade form FIR filter structure system generator model.

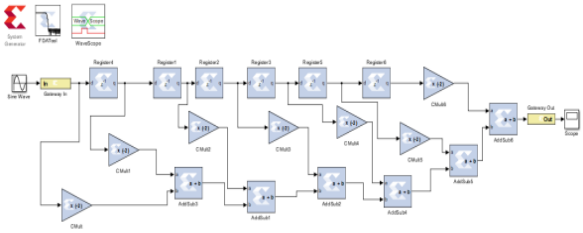

Figure 3: System Generator model for Direct form FIR filter structure.

$$H(z) = 0.0886((1 + 1.8233\,z^{-1} + z^{-2})(1 + 0.6141z^{-1} + z^{-2})(1 - 0.8793z^{-1} + z^{-2})) \quad (3)$$

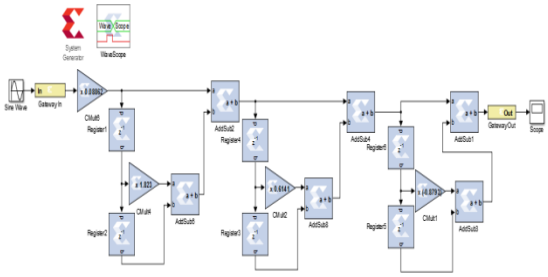

Figure 4: System Generator model for Cascade form FIR filter structure

4.3 Implementation of Frequency Sampling form FIR Filter Structure

On the unit circle, this form may be used to reconstruct the system function H(z). The parallel structure described in (4), System Generator model for the frequency-sampling form FIR filter structure illustrated in **Figure 5**, is the result of the system function in (2).

$$H(z) = \frac{1 - z^{-7}}{7}\begin{bmatrix} 0.3724\,\dfrac{-0.901 + z^{-1}}{1 - 1.247z^{-1} + z^{-2}} \\ +0.0548\,\dfrac{-0.6235 + 0.6235z^{-1}}{1 + 0.445z^{-1} + z^{-2}} \\ +0.0119\,\dfrac{-0.2225 + 0.2225z^{-1}}{1 + 1.8019z^{-1} + z^{-2}} \\ +0.9928\,\dfrac{1}{1 - z^{-1}} \end{bmatrix} \quad (4)$$

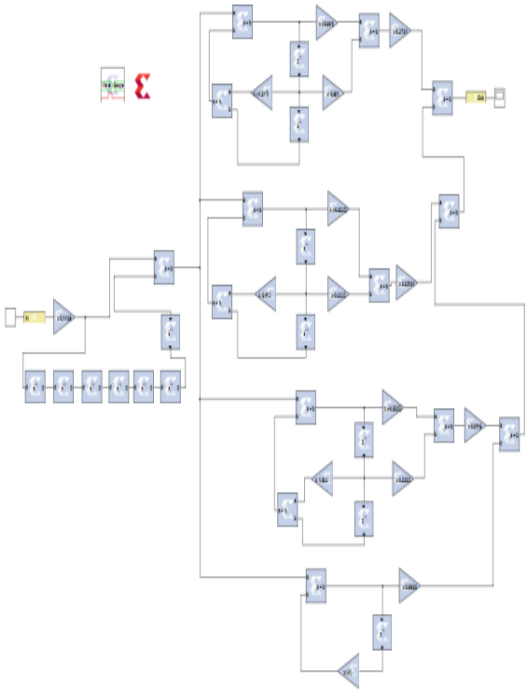

Figure 5: System Generator model for Frequency-sampling form FIR filter structure.

4.4 Implementation of Lattice FIR Filter Structure

The lattice filter coefficients may be calculated using the system function H(z) in (2). **Figure ٦** depicts the system generator model for the lattice FIR filter construction.

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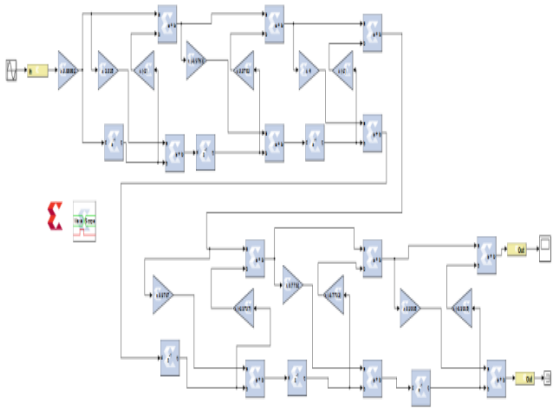

Figure ٦: System Generator model for Lattice FIR filter structure.

٥ The Implementation Result

The hardware resources required to imlplement the four structures on Artix-7 FPGA kit are illustrated in Table 1.

From Table ١, the hardware area by the Four FIR filter structures are approximately similar. Also the hardware area by the FIR filter structures are efficient in hardware area they belong to the implementation with System Generator tools from The MathWorks.

6 Conclusions

In this paper, different structures of the 6th FIR filter are presented and implemented on XC7A100T-1CSG324C Artix-7 FPGA kit with flexibility and less complexity. Utilizing System Generator tools from the MathWorks has the additional advantage of allowing fast study and investigation of various implementation techniques. As a future work, the IIR filter structures can be introduced and implemented to be compared with the FIR filter structures.

Table 1: The implementation results of FIR filter structures.

Structure	Resource	Used	Available	Utilization ratio
Direct Form	Number of occupied Slices	**102**	**15850**	**1%**
	Number of Slice Registers	**75**	**126800**	**1%**
	Number of Slice LUTs	**81**	**63400**	**1%**
Cascade	Number of occupied Slices	**174**	**15850**	**1%**
	Number of Slice Registers	**127**	**126800**	**1%**
	Number of Slice LUTs	**505**	**63400**	**1%**
Frequency -sampling	Number of occupied Slices	**422**	**15850**	**2%**
	Number of Slice Registers	**339**	**126800**	**1%**
	Number of Slice LUTs	**1212**	**63400**	**1%**
Lattice	Number of occupied Slices	**343**	**15850**	**2%**
	Number of Slice Registers	**117**	**126800**	**1%**
	Number of Slice LUTs	1110	63400	**1%**

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Biography

Rasha Waleed was born in Mosul, Nineveh, Iraq, in 1987. She received B.S. and M.Sc. degrees in Electrical Engineering from Mosul University, in 2008, and 2012, respectively. she is work as assistant lecturer in Technical Computer Engineering, Al-Hadba University College, Mosul, IRAQ. She has many researches in the field of digital signal processing with different applications.

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