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Study the Effect of Switching Frequency on THD of Multilevel Inverter

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Abstract: This study looks at a single phase nine level inverter with asymmetrical cascaded H-Bridge multilevel inverter topology that requires fewer components when compared to other techniques MATLAB Simulink has been used to create and model inverters with various switching frequencies. Observe the effect of total harmonic distortion (THD) without and with a passive filter. The power circuit for the asymmetrical cascaded H-bridge multilevel inverter is controlled using a sinusoidal pulse width modulation (SPWM) technique. The THD is used to compare the efficacy.

Keywords: *MLI, THD, SPWM, CHB.*

1 Introduction

Multilevel inverters (MLIs) are gaining popularity in a variety of industrial and renewable energy applications these days. MLIs have improved power quality and less total harmonic distortion (THD) as compared to their two-level competitors. In industries, conventional MLI topologies such as flying capacitor MLI, neutral point clamped MLI, and cascaded H-Bridge (CHB) MLI are utilized for a variety of applications. Solar PV systems, wind energy systems, and railway traction are examples of high-power applications, while MLI is utilized in pumps, conveyor belts, grinding mills, turbine starters, and marine propulsion (Kouro et al., 2010; Abu-Rub et al.,2010; Akagi, 2017; Leon et al.,2017). However, these traditional topologies, have inherent drawbacks. In the CHB architecture, the number of isolated DC power supplies required increased with the number of levels in voltage output waveform, whereas the FC-MLI structure necessitates a complicated control system to maintain a steady voltage across the capacitor. Increasing the number of capacitors exponentially with the increasing output voltage level led to control becoming more difficult. The research has concentrated on designing topologies to address the drawbacks of the traditional multilevel voltage source inverter (VSI) over the last few years (Venkataramanaiah et al.,2017; Vijeh et al.,2019).

By increasing the number of levels at the output voltage, researchers are seeking to increase the quality of the output voltage waveform while decreasing the number of switches to overcome the cost limitation. The advantages of the architecture with a higher number of levels are increased reliability, efficiency, reduced filter size, power density, and other applications (Gupta et al.,2016).

The motivation for developing improved MLI topologies is to reduce the number of DC supplies, switches, and gate drivers required. Several topologies have been proposed in the literature based on these factors (Vijeh et al.,2019; Gupta et al.,2016; Prabaharan and Palanisamy, 2017).

In (Alishah et al.,2016) the output voltage waveform in a topology depends on a designed H-bridge provides negative polarity and positive polarity. However, because the topology requires two switches to block the maximum output voltage, it can't be used for high-voltage applications. The authors of (Alishah et al.,2017) attempted to deal with this problem by changing the topology of the circuit. Several alternative MLI topologies have been presented in (Siddique et al.,2018; Sabyasachi et al.,2017; Dhanamjayulu, and Meikandasivam, 2018;

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Seifi et al.,2019; Mohamed, et al.,2019) each with its own set of benefits and drawbacks.

The topology presented in (Babaei, 2008) features a structure that can be coupled in series as a sub-multilevel module. The use of a backend H-bridge, however, limits its applicability in high-voltage applications has been updated and a revised topology is presented in (Ebrahimi, et al.,2012). The half-bridge configured dc sources are used in the cascaded topology instead of dc sources, switches are used in one leg of the modified single unit structure, and each unit has its H-bridge for determining voltage polarity. Due to the cascade connection, the redesigned structure places less voltage stress on the H-bridge switches, however, the number of switches rises in comparison to (Babaei, 2008). The (Samsami, et al., 2017) suggested a multilevel bidirectional inverter design with asymmetric and symmetric configurations that require less DC power supplies, power electronics switches, and driver circuits, However, the overall standing voltage of the topology is increased by using a backend H-bridge.

Various topologies have used modified H-Bridge configurations to increase the level of inverter output (Babaei et al.,2014; Jayabalan et al.,2017; Gautam et al.,2016; Babaei and Laali, 2015; Shalchi and et al.,2017; Samadaei and et al.,2016; Samadaei and et al.,2018). A Modified H-Bridge generates an output inverter level corresponding to the addition of the output inverter on the two sides of the Modified H-Bridge in addition to the polarity of the voltage level. At least two switches are required to block the output voltage peak in all of the above topologies. Similarly, the lower voltage stress across the switches has given rise to a new type of multilevel inverter topologies. The maximum voltage stress that can be applied to any switch in this topology is less than the maximal output voltage (Siddique and et al.,2019; Thiyagarajan, 2019; Noman and et al.,2018; Gupta and Jain, 2014; Rawa and et al.,2019).

This paper will study the effect of THD by varying the switching frequency of SPWM on the output of nine level inverter with resistive load and with an LC filter

2 Investigation of Nine Level VSI

Figure 1 shows the investigated topology for 9-level VSI output, which includes two different DC sources and eight switches. By operating the electronic circuit according to the sequences of switching in Table 1 the voltage output of the circuit will be nine level waveforms.

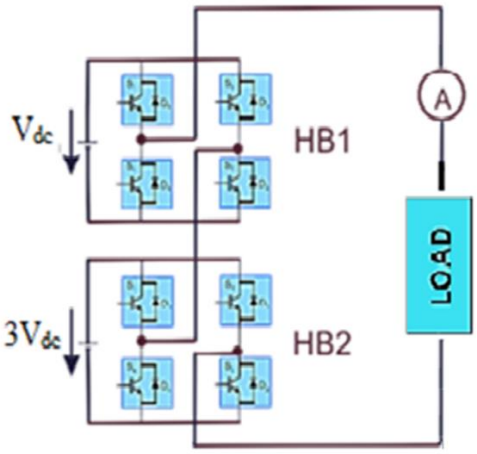

Figure 1: Nine Level VSI Topology

In Figure 1 we used asymmetrical CHB circuit to implement a smaller number of switches and a greater number of levels were used only two H- bridge.

Table 1: The switching sequence of nine level inverter

Output voltage	S1	S2	S3	S4	S5	S6	S7	S8
100 V	ON	OFF	OFF	ON	ON	OFF	OFF	ON
75 V	ON	ON	OFF	OFF	ON	OFF	OFF	ON
50 v	OFF	ON	ON	OFFF	ON	OFF	OFF	ON
25 v	ON	OFF	OFF	ON	ON	ON	OFF	OFF
0 v	ON	ON	OFF	OFF	ON	ON	OFF	OFF
-25 v	OFF	ON	ON	OFF	ON	ON	OFF	OFF
-50 v	ON	OFF	OFF	ON	OFF	ON	ON	OFF
-75 v	ON	ON	OFF	OFF	OFF	ON	ON	OFF
-100 v	OFF	ON	ON	OFF	OFF	ON	ON	OFF

3 Sinusoidal Pulse Width Modulation Method

Different modulation approaches have been used to control the output of voltage waveforms in multilevel inverters. Low and high switching frequency control approaches are the most common classifications for these control systems. Low switching approaches such as Selective Harmonic Elimination and Space Vector Control commutate the active power switch just one or two times each cycle. However, on the other side, for high switching approaches in which the power switch is switched numerous times within a cycle, various PWM are employed (Boussada et al., 2017 ; Al-Badrani, 2022; Saleh et al., 2021). In this study SPWM has been used

to operate nine level inverters at varying switching frequencies.

The SPWM is the most widely utilized control method for multilevel inverter control, according to authors in the literature. By contrasting a triangular carrier waveform with a sinusoidal reference waveform, the control pulses are produced, as shown in Figure (2). The carrier frequency of the triangle carrier waveform is fc, while the peak-to-peak amplitude is Ac. The carrier signal's frequency determines the inverter's switching frequency and the output voltage's high order harmonic component (Pamujula et al.,2020). The sinusoidal modulation signal, on the other hand, will have a low frequency fr and a peak-to-peak amplitude of Ar. The needed line voltage frequency at the inverter's output is determined by the frequency of the sinusoidal modulation waveform, and its amplitude regulates the modulation index Missss (Colak et al., 2011). In the case of inverter control with many levels a single reference waveform signal and multi-carrier triangular waveforms should be used. During the control procedure, every time a carrier signal is evaluated, it is compared to the reference waveform. A string of pulses is generated as a result of this comparison, which controls the power switches. When the reference waveform exceeds the carrier signal associated with that switch, the active power switch turns on.

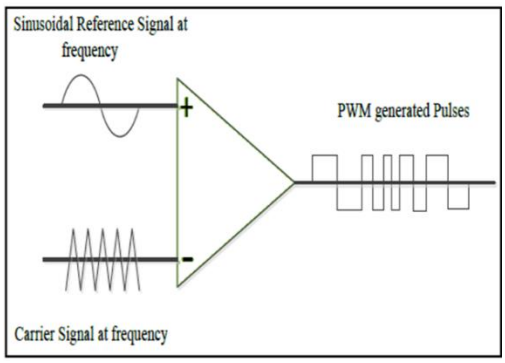

Figure 2: Basic principle of PWM method

4 Simulation Results

The proposed system's simulation is achieved with the help of MATLAB software. First, a simulation of the suggested multilevel inverter is performed. The switching scheme shown in Table 1 is used to provide pulses to each switch. A nine-level inverter has been implemented with four states depending on the frequency change.

4.1 Case 1. At 5 kHz switching frequency

Figure 3(a) displays the voltage wave at 5 kHz switching frequency without the use of passive filter, whereas Figure 3(b) shows the spectrum and THD of the same wave. However, the voltage wave becomes smoother when the filter is applied at the same frequency as shown in Figure 4(a), and THD drops from 14.15 to 10.79 as shown in Figure 3(b) and Figure 4(b).

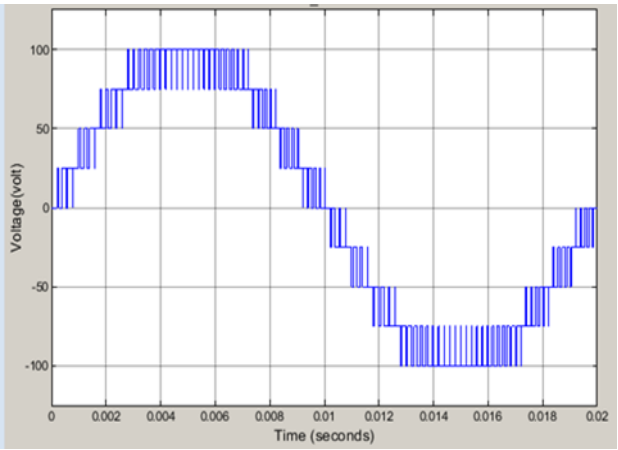

Figure 3(a): output inverter without filter at 5KH switching frequency

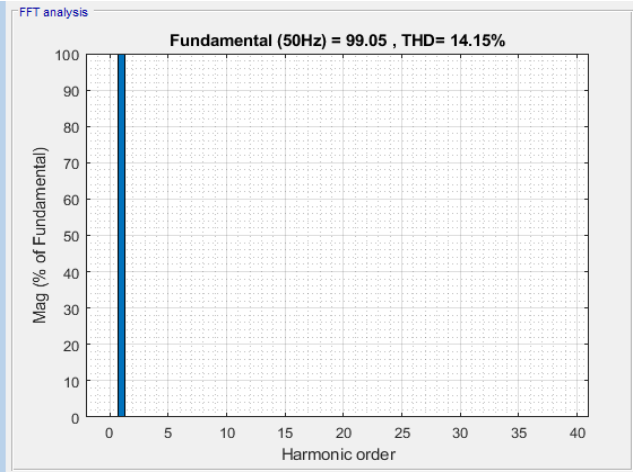

Figure 3(b): THD without filter at 5 kHz switching frequency

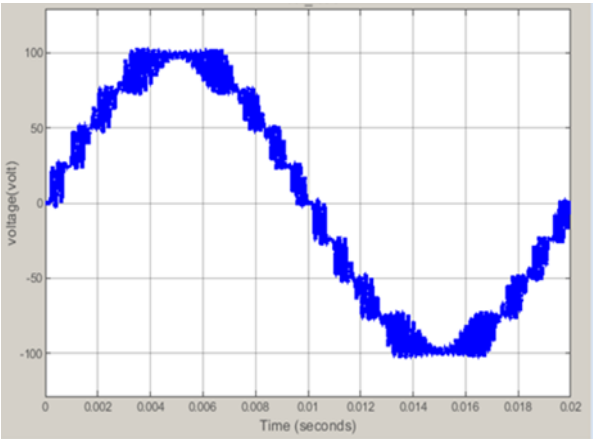

Figure 4(a): Output inverter with filter at 5 kHz switching frequency

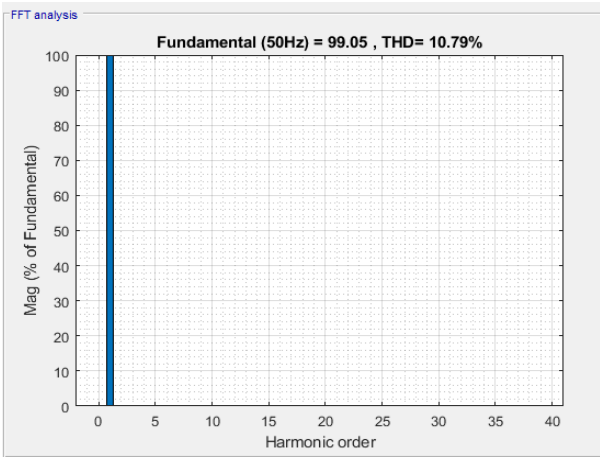

Figure 4(b): THD with filter at 5 kHz switching frequency

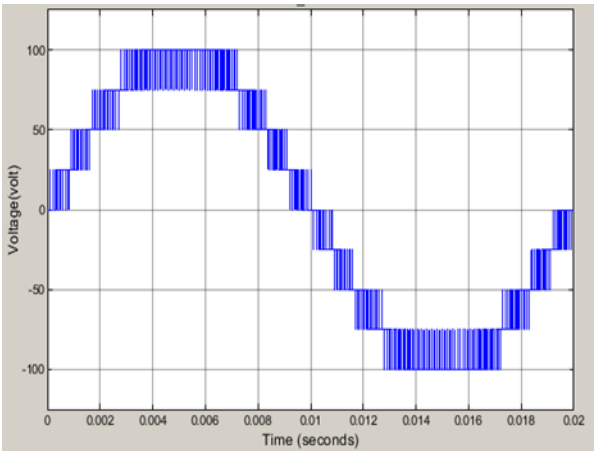

Figure 5(a): 9_Levelinverter output voltage without filter at 10 kHz switching frequency

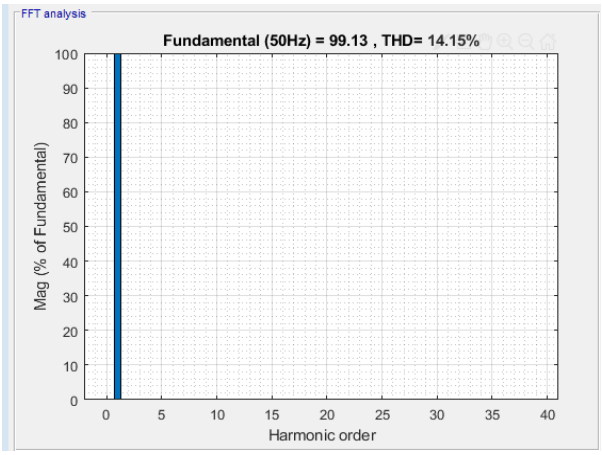

Figure 5(b): THD without filter at 10 kHz switching frequency

4.2 Case 2. At 10 kHz switching frequency

Figure 5(a) displays the voltage wave at 10 kHz switching frequency without the use of a filter, whereas Figure 5 (b) shows The THD of the same wave. However, the voltage wave becomes smoother when the filter is applied at the same frequency as shown in Figure 6(a), and THD drops from 14.15 to 4.34 as shown in Figure 5(b) and Figure 6(b). When compared with case 1 by increasing a switching frequency from 5kHz to 10 kHz, we notice no change in THD with no filter, however we detect a huge difference in THD with the filter, where the THD dropped down for you from 10.79 to 4.34.

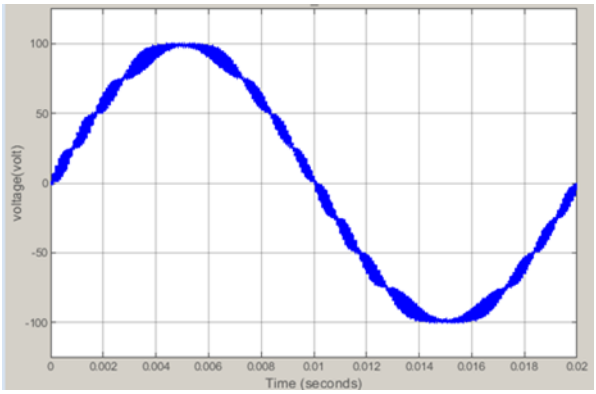

Figure 6(a): 9_Level inverter output voltage with filter at 10 kHz switching frequency

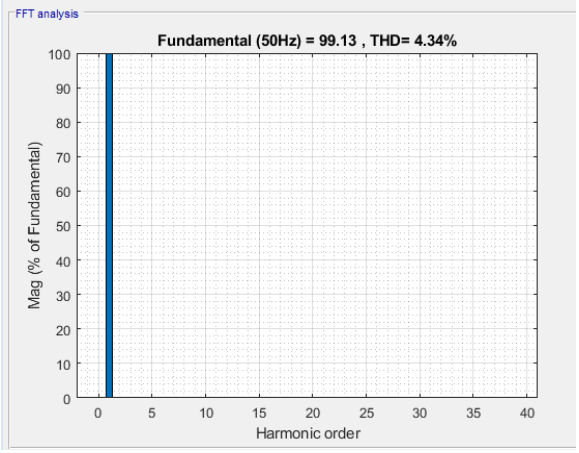

Figure 6(b): THD with filter at 10 KH switching frequency

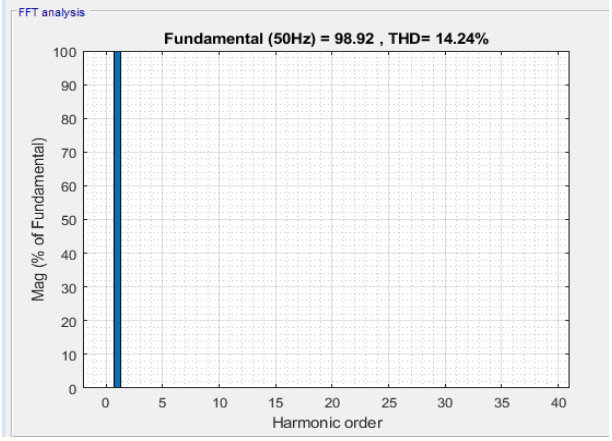

Figure 7(b): THD without filter at 15 KH switching frequency

4.3 Case 3. At 15 kHz switching frequency

Figure 7(a) displays the voltage wave at 15 K switching frequency without the use of a filter, whereas Figure 7(b) shows The THD of the same wave. However the voltage wave becomes smoother when the filter is applied at the same frequency as shown in Figure 8(a), and THD drops from 14.24 to 1.92 as shown in Figure 7(b) and Figure 8(b).When compared with case 2 by increasing a switching frequency from 10k to 15k, we notice little change in THD with no filter from 14.15 to 14.24, however we detect a difference in THD with the filter, where the THD dropped down for you from 4.34 to 1.92.

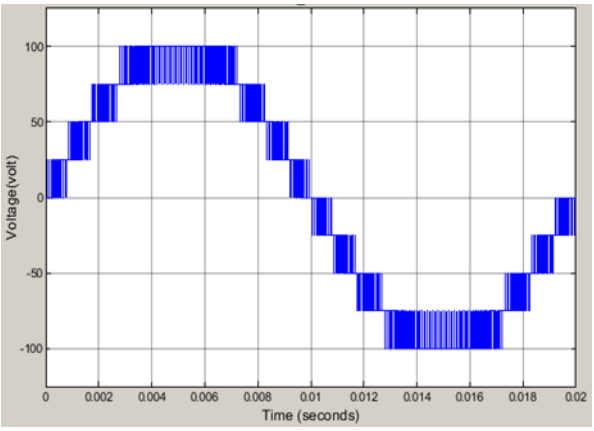

Figure 7(a): output inverter without filter at 15KH switching frequency

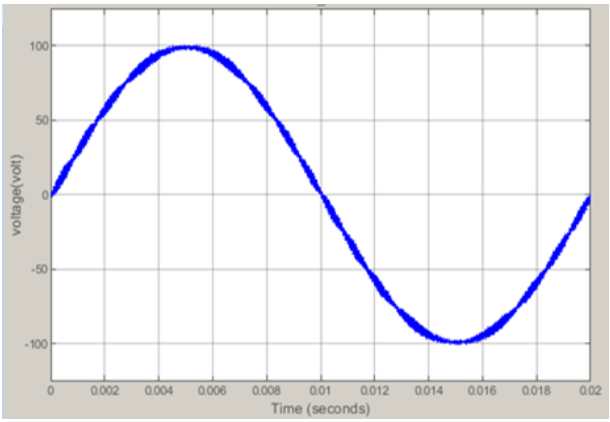

Figure 8(a): output inverter with filter at 15KH switching frequency

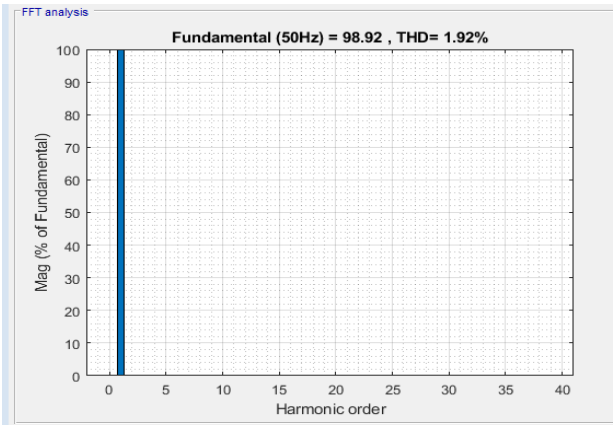

Figure 8(b): THD with filter at 15 KH switching frequency

4.4 Case 4. At 20 k switching frequency

Figure 9(a) displays the voltage wave at 20K switching frequency without the use of a filter, whereas Figure 9(b) shows The THD of the same wave. However, the voltage wave becomes smoother when the filter is applied at the same frequency as shown in Figure 10(a), and THD drops from 14.24 to 1.07 as shown in Figure 9(b) and Figure 10(b). When compared with case 3 by increasing a switching frequency from 15k to 20k, we notice no change in THD with no filter, however we detect a difference in THD with the filter, where the THD dropped down for you from 1.92 to 1.07.
Table 2 show the THD change with various switching frequency with filter and without filter.

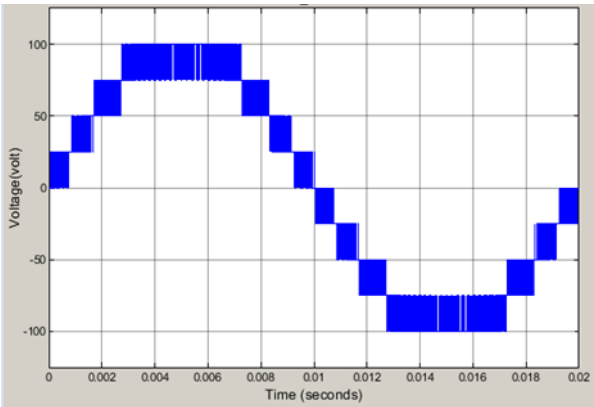

Figure 9(a): output inverter without filter at 20KH switching frequency

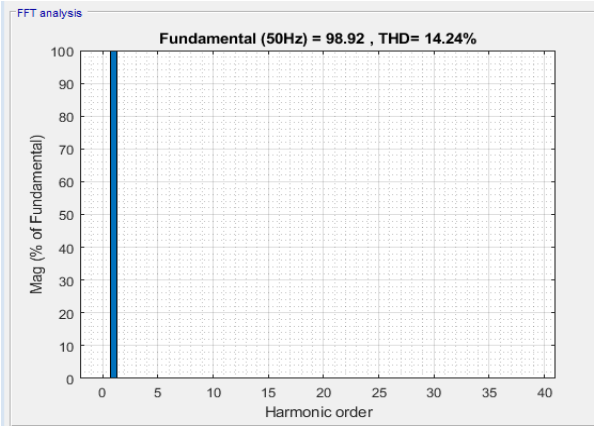

Figure 9(b): THD without filter at 20 KH switching frequency

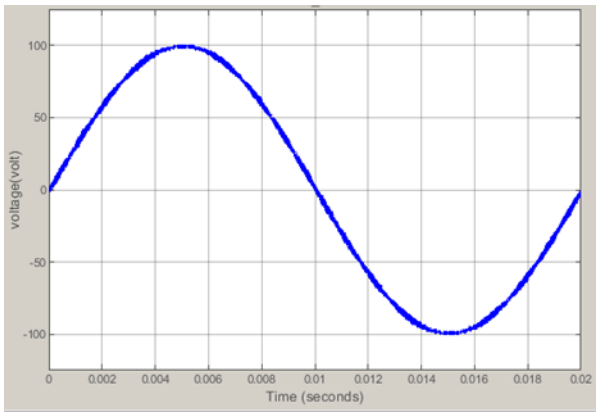

Figure 10(a): output inverter with filter at 20KH switching frequency

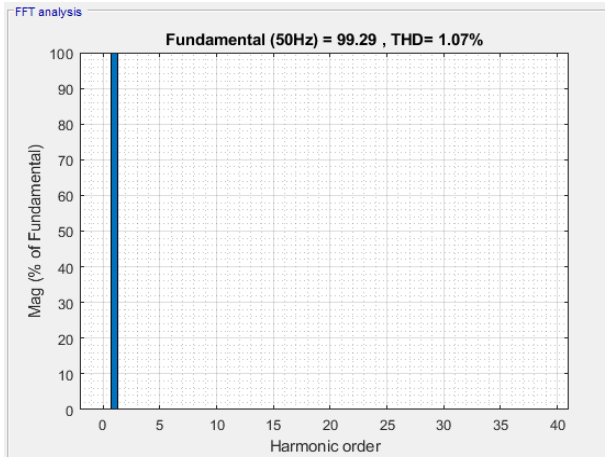

Figure 10(b): THD with filter at 20 KH switching frequency

Table 2: THD change with various switching frequency with filter and without filter.

Switching frequency	5k	10k	15k	20 k
THD Without filter	14.15%	14.15%	14.24%	14.24%
THD With filter	10.79%	4.34%	1.92%	1.07%

5 Conclusions

The THD of single phase nine level inverter output voltage with a passive filter at switching frequencies of 5kHz, 10kHz, 15kHz, and 20kHz are found to be 10.79%, 4.34%, 192%, and 1.07 % respectively. It indicates that as the switching frequency increased, the percentage of THD reduced abruptly. However, The THD of nine level inverters without a filter at 5kHz, 10kHz, 15kHz, and 20kHz are found to be 14.15%, 14.15%, 14.24%, and 14.24 %. It indicates that as the switching frequency increased, the percentage of THD stay constant or had little change. As the switching frequency of an inverter with a filter is increased, the harmonic distortion is reduced. As a result, in terms of THD content, the performance of the MLI is dependent on switching frequency.

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APPENDICES

Design of the Output Filter

LC filter as demonstrated in figure (3.2) is used in the simulation to suppress the high harmonics and improve the generated waveform. The inductor and the capacitor work as energy storage therefore they increase the efficiency of the inverter. Moreover, values of L and C determine the filter performance and the cut-off frequency. So, they need to be chosen carefully to avoid resonant frequency in addition to achieve best performance (Texas Instruments Incorporated, 2022).

Inductor Design

The value of the inductor is calculated by the following equation

$$L = \frac{V_{DC}}{Num\ of\ Levels \times f_{sw} \times I\max \times ripple_{percentage}}$$

Where:
fsw: the switching frequency.
Ripple percentage is the inductor ripple current to be selected at 40% of the RMS current of the inverter which is considered in most of references
By substituting the values L is calculated as following

Capacitor Design

To assign the capacitor value, it is calculated by equation

$$C = \frac{\%Q_{rated}}{2\pi \times f_{Load} \times V_{Load}^2}$$

Where % Qrated is the total reactive power absorbed by the capacitor which is limited by 5% of the total power for each phase. fLoad is the generated frequency, VLoad is the voltage of generated waveform.

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